

Fig. 1 (PRIOR ART)

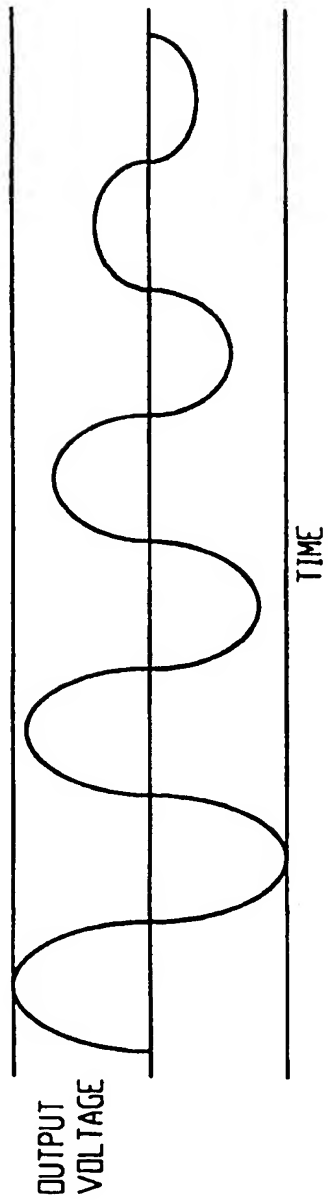


Fig. 3

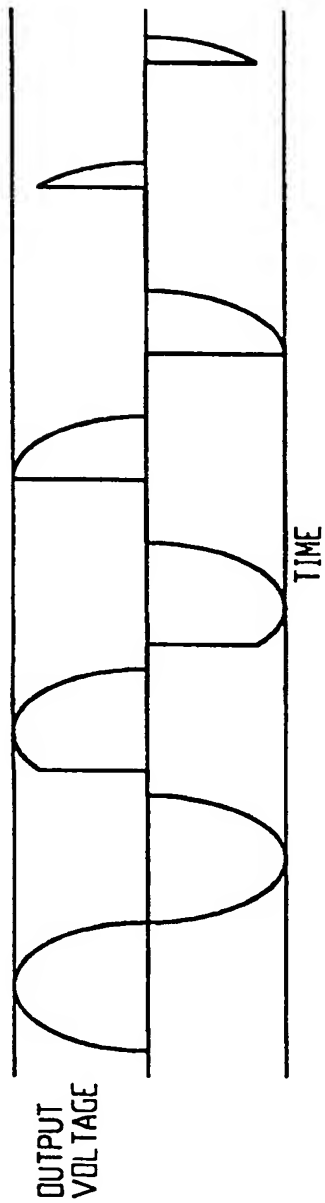


Fig. 2

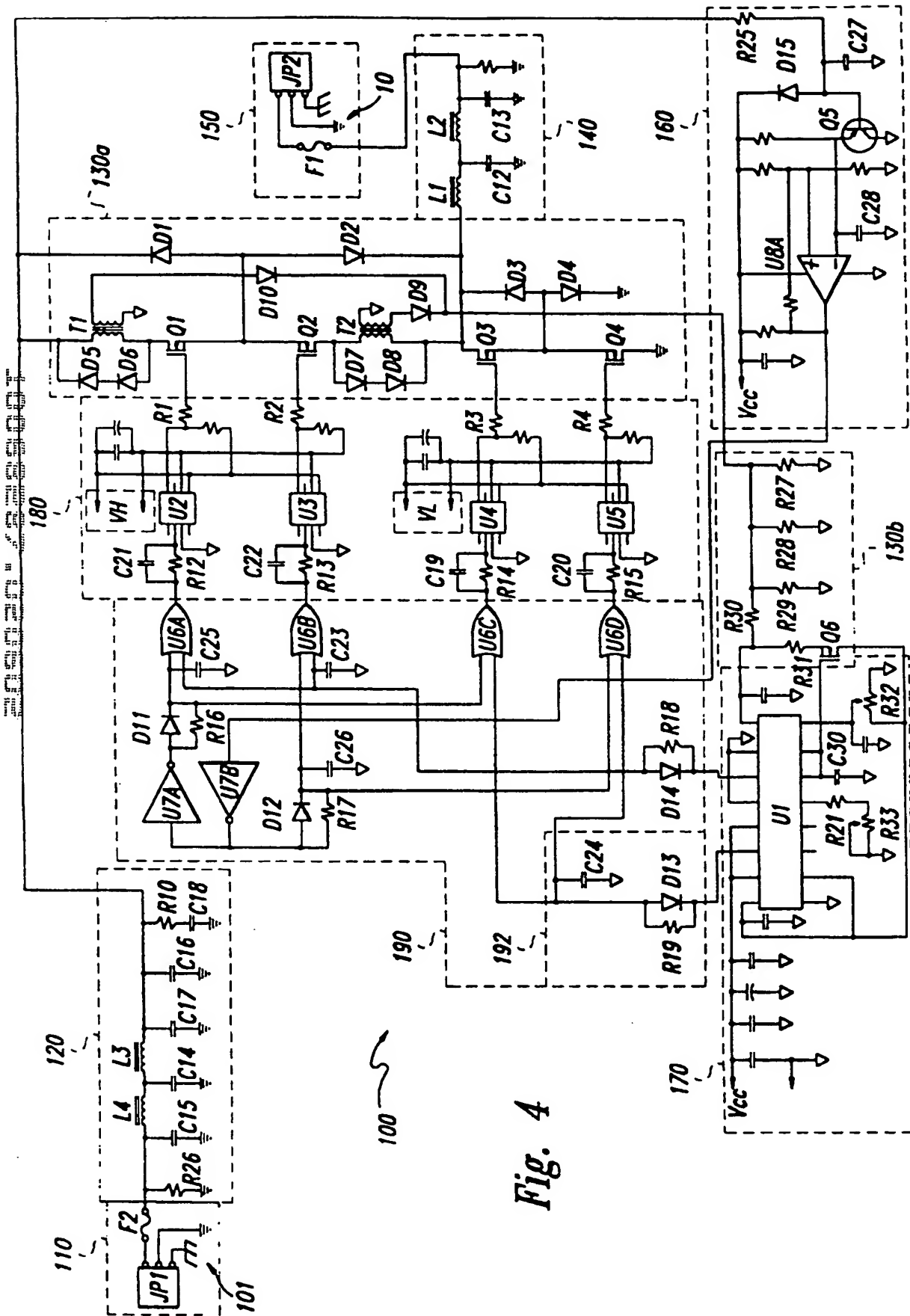


Fig. 4

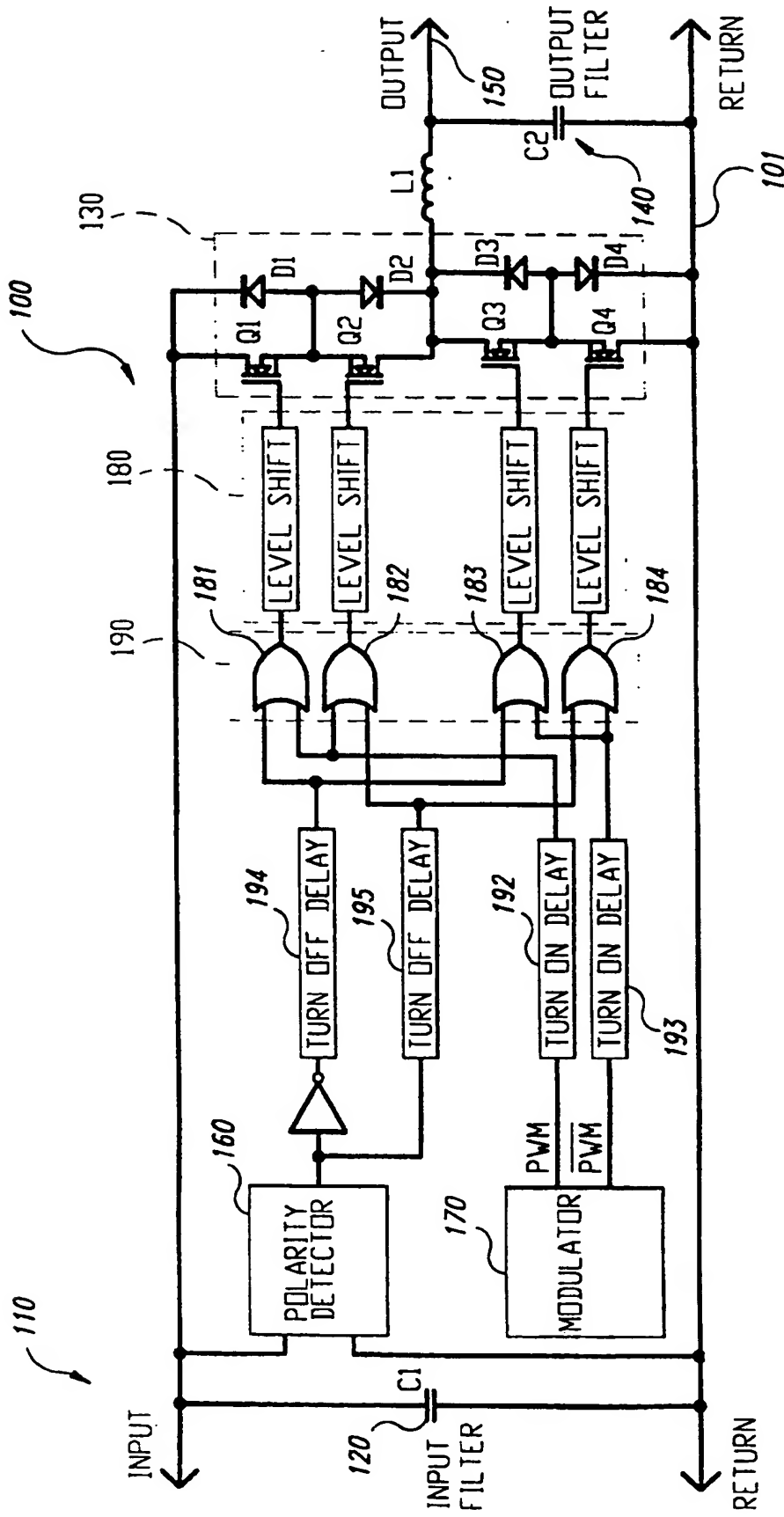


Fig. 5

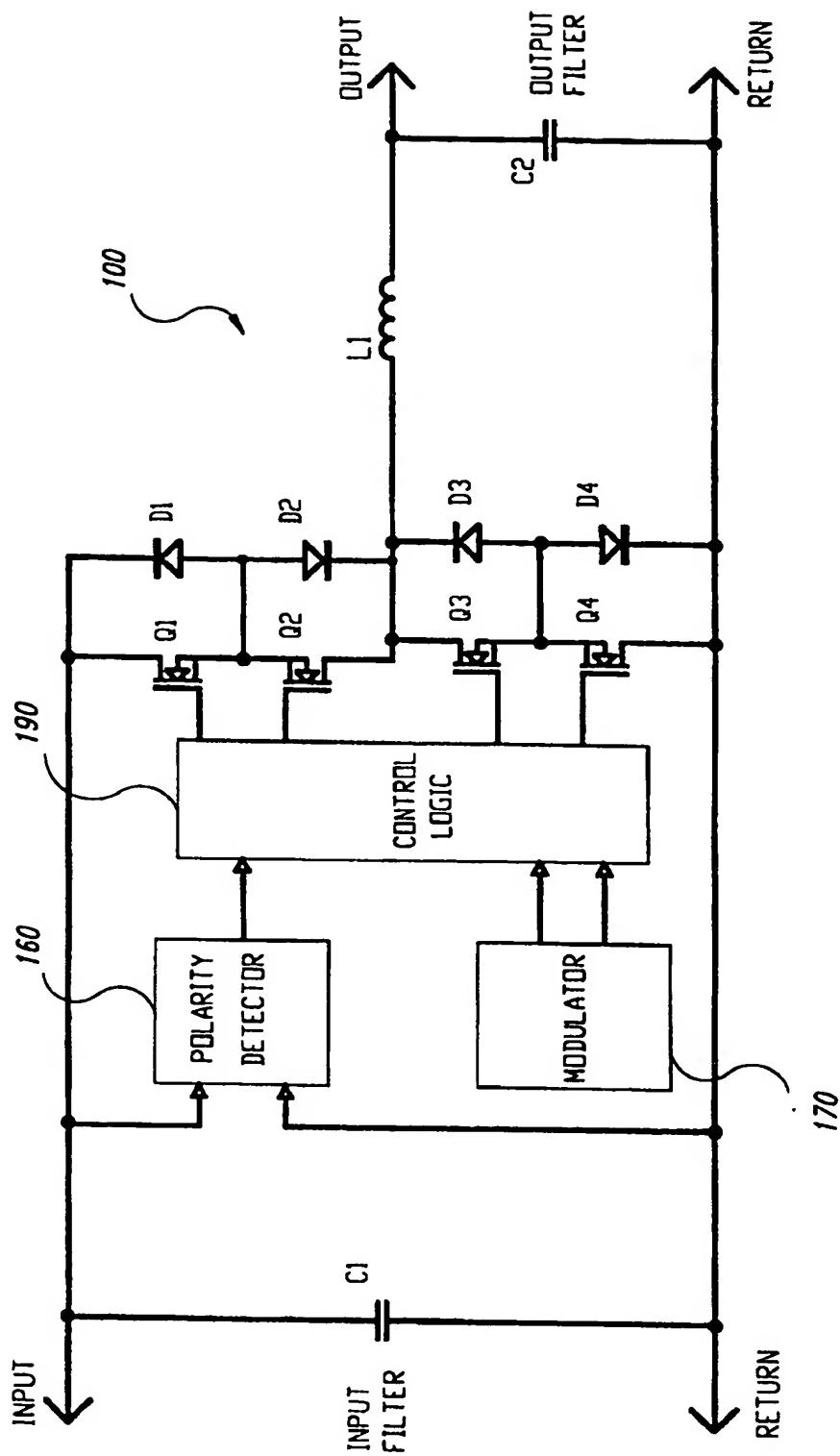


Fig. 6A

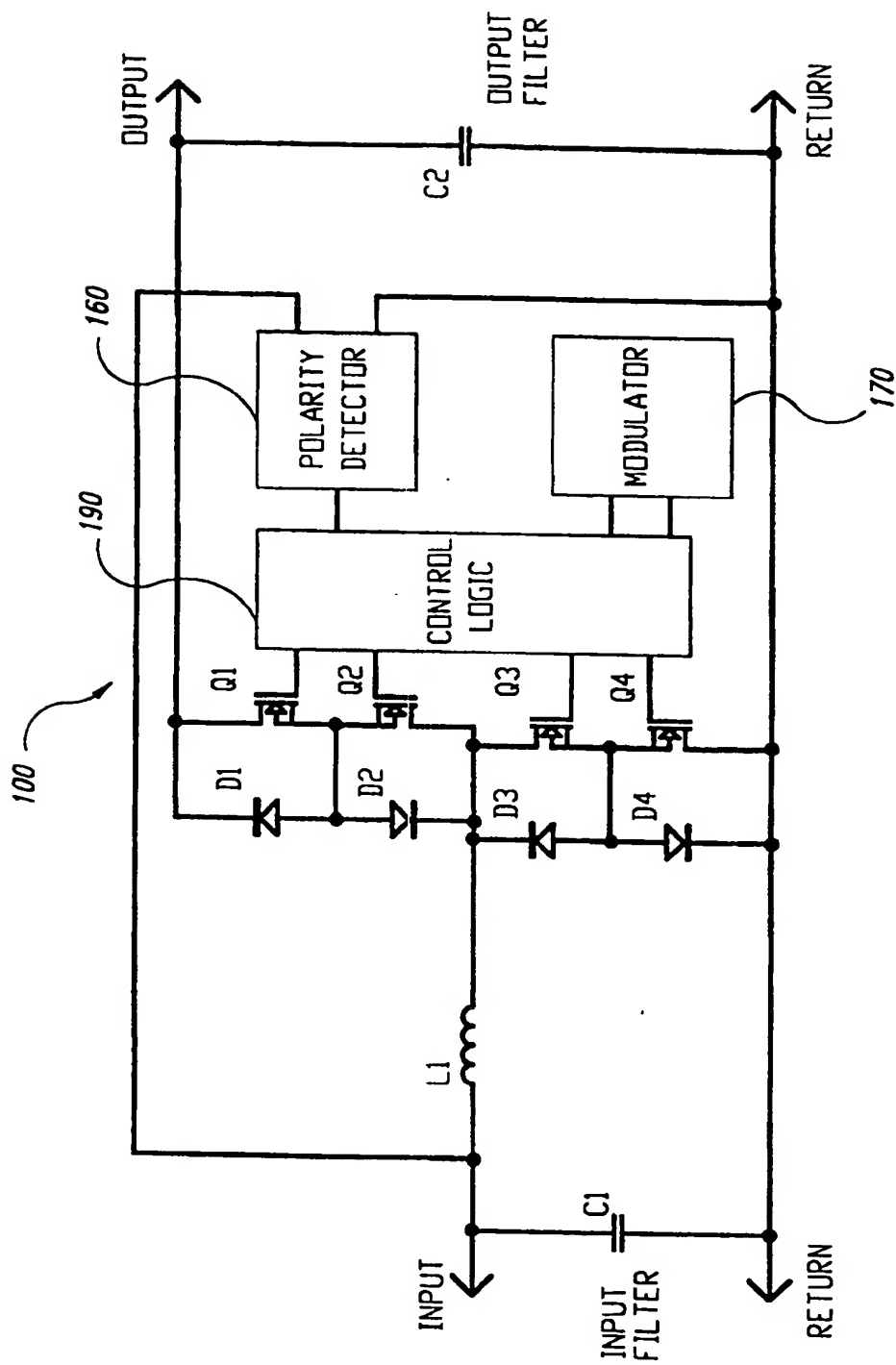
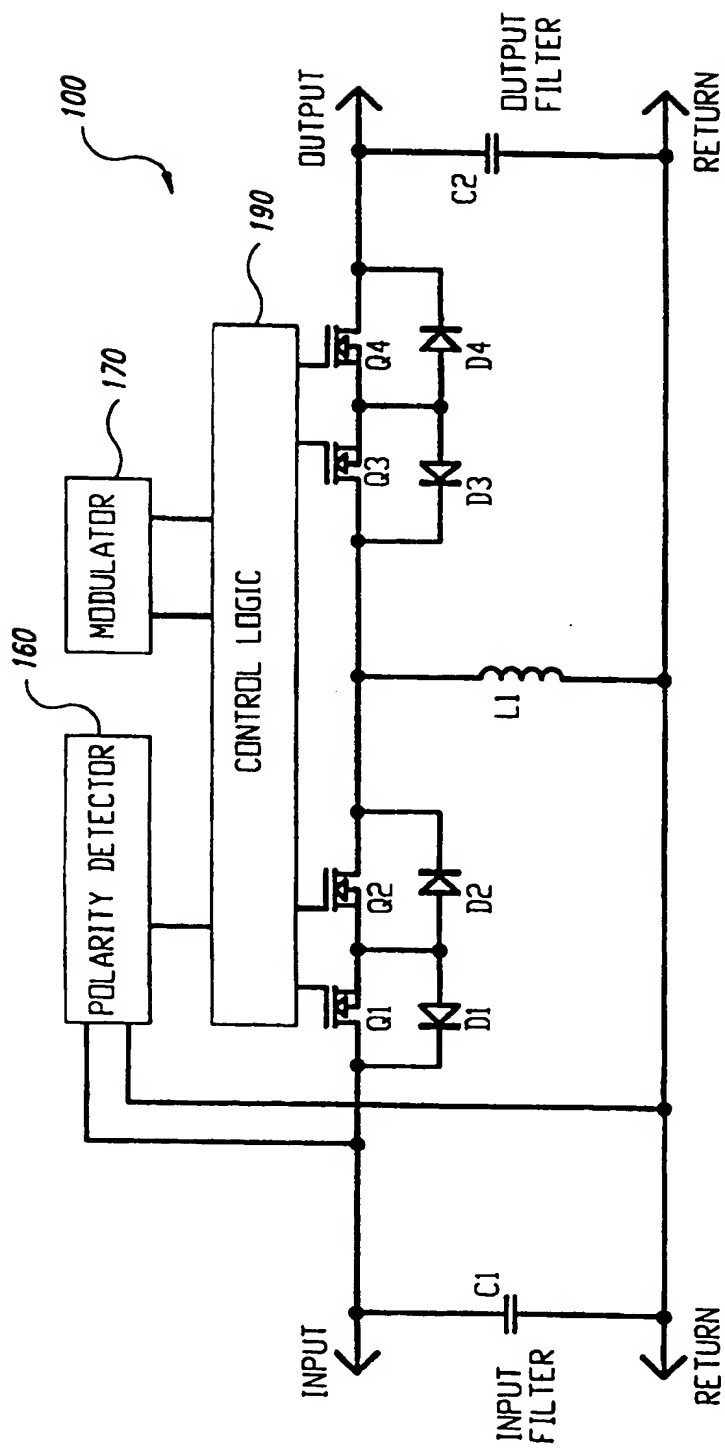


Fig. 6B



*Fig. 6C*

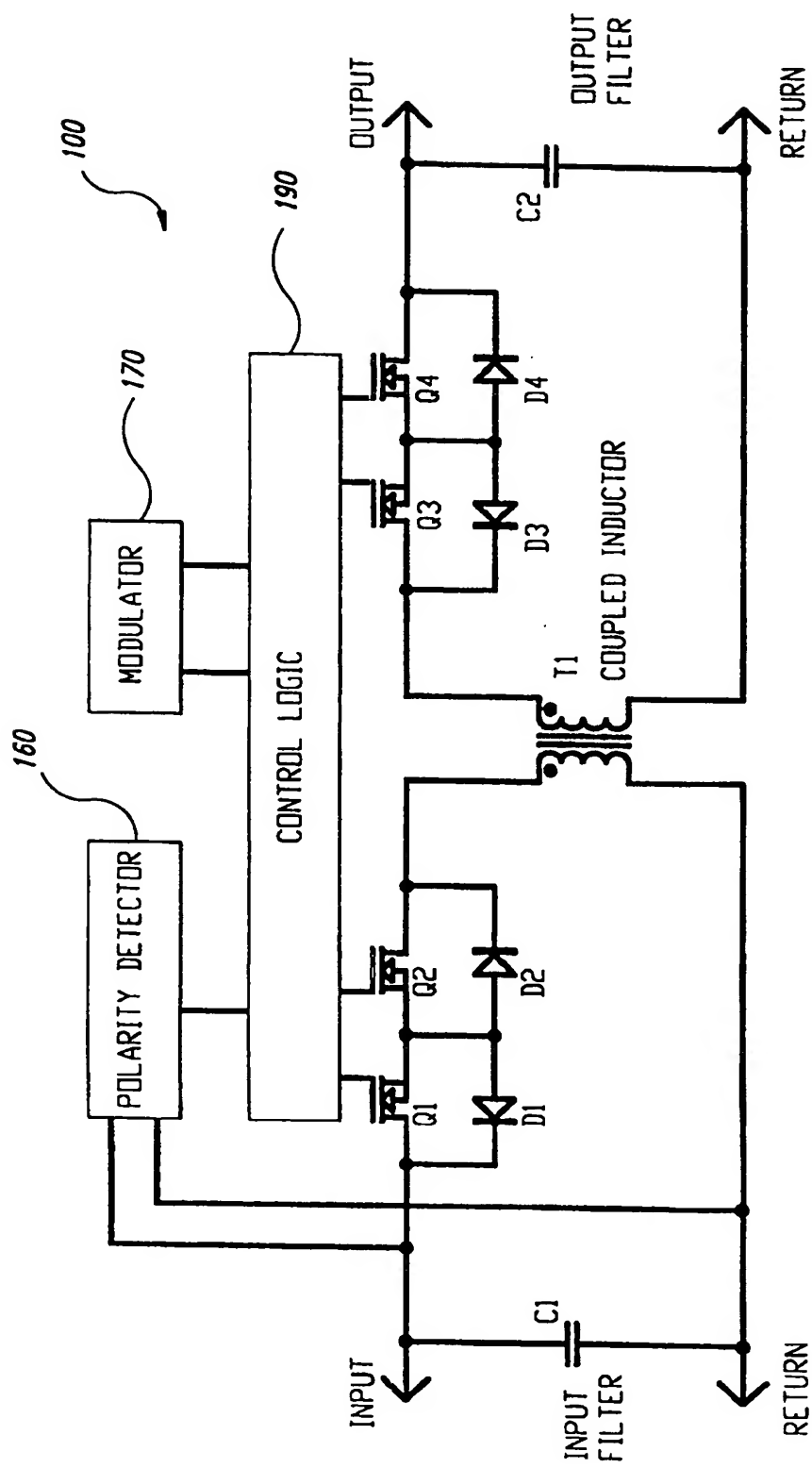
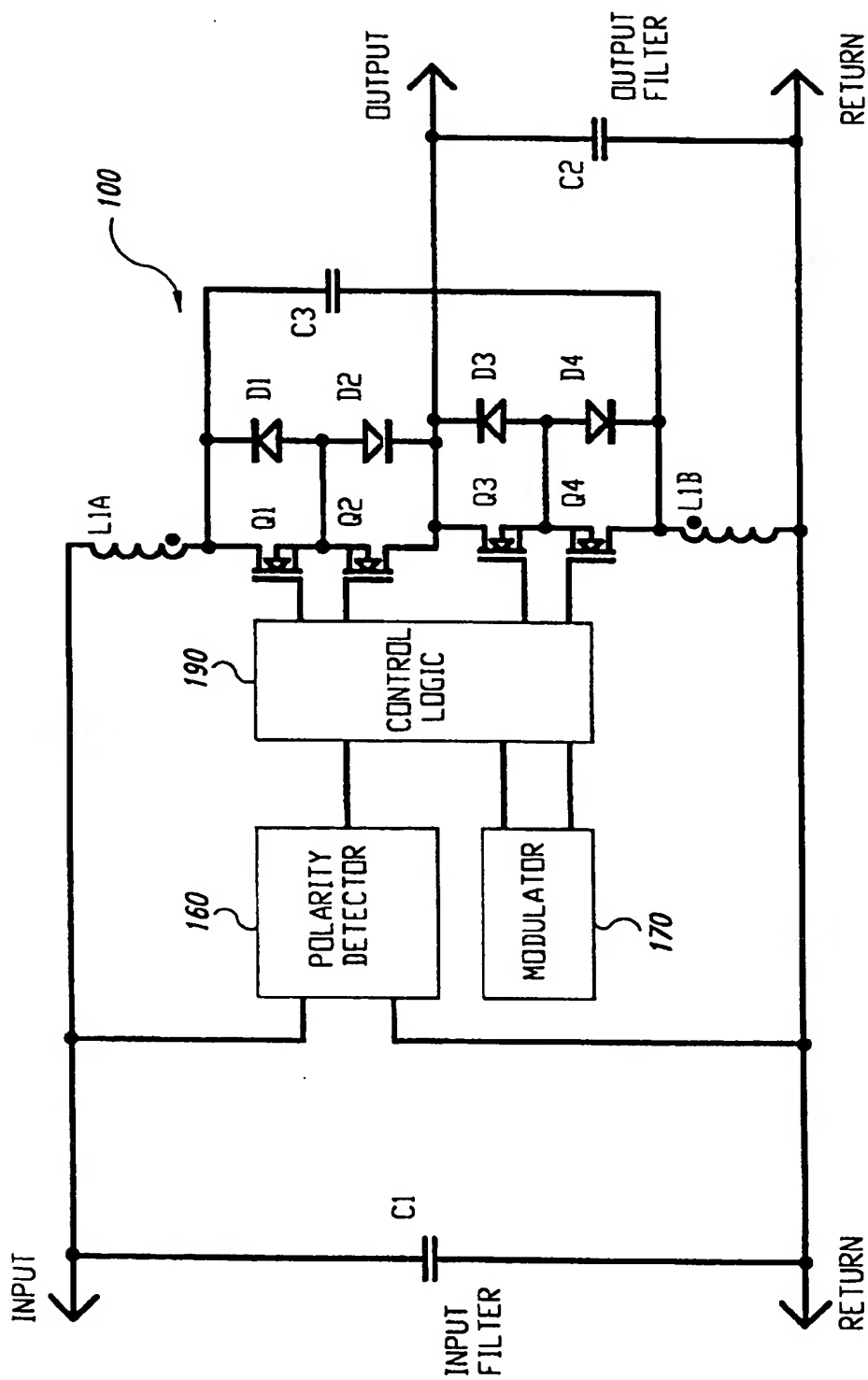


Fig. 6D





**Fig. 7A**

FIG. 7B is a schematic diagram of a power supply circuit.

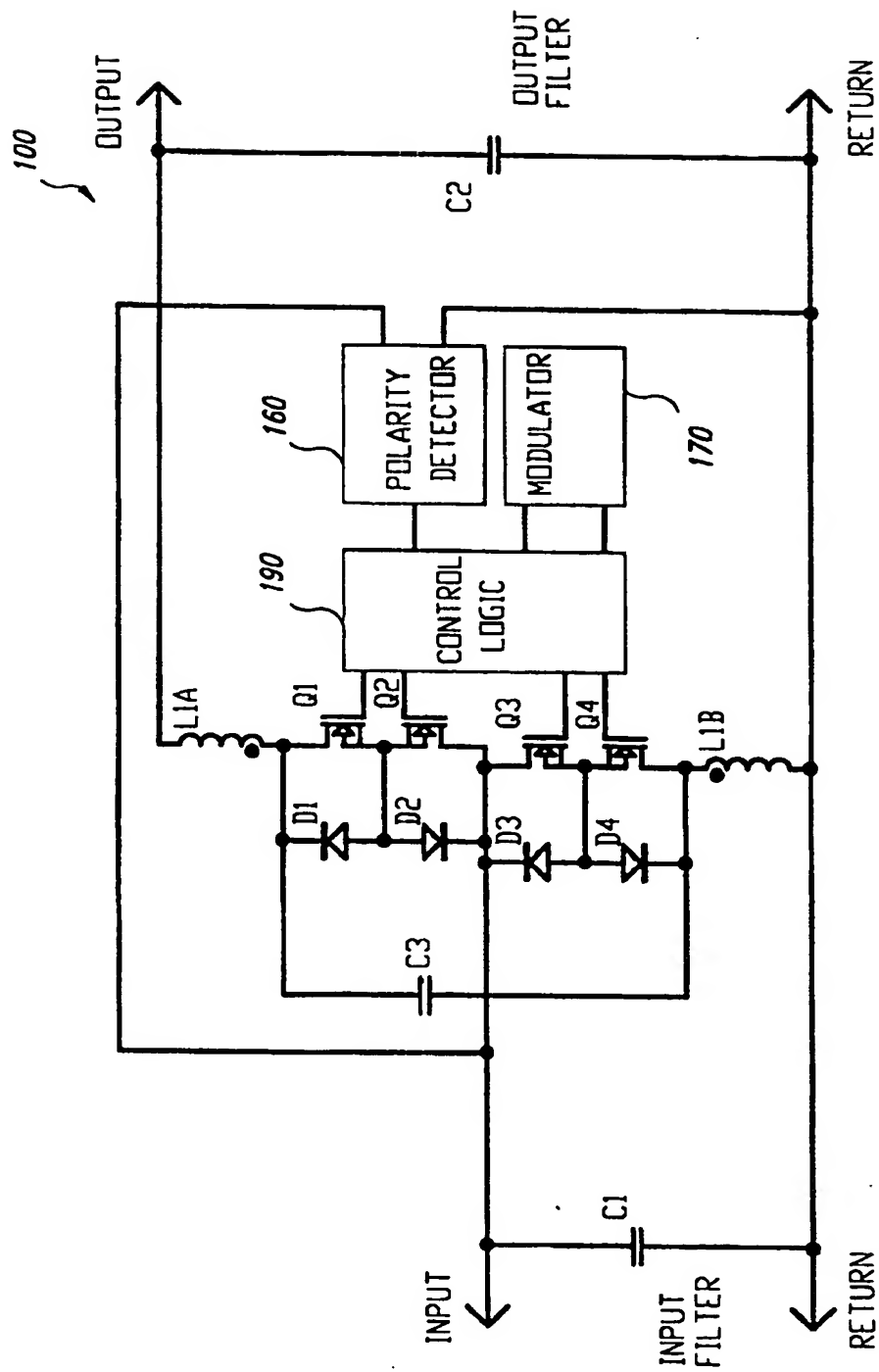


Fig. 7B

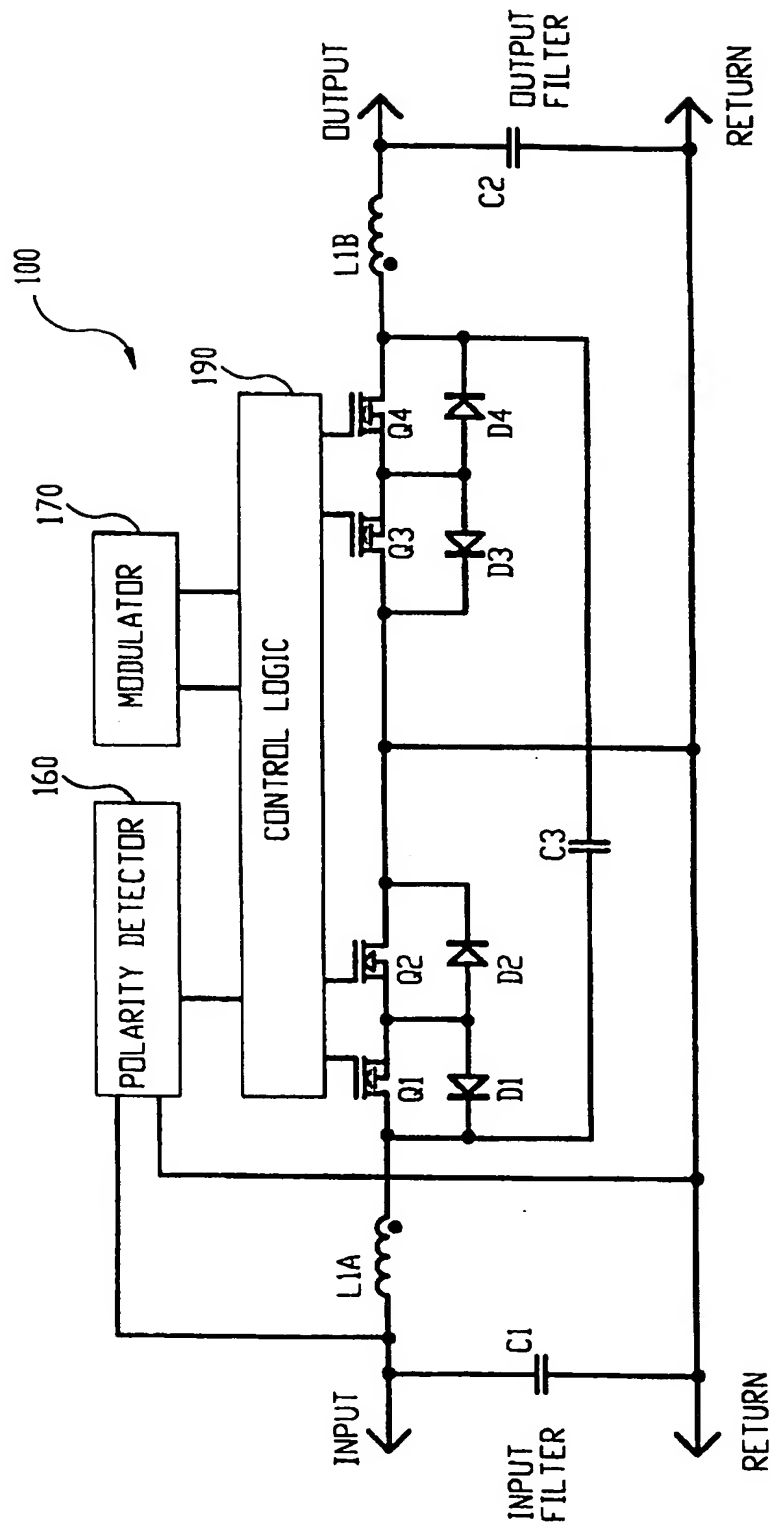


Fig. 7C

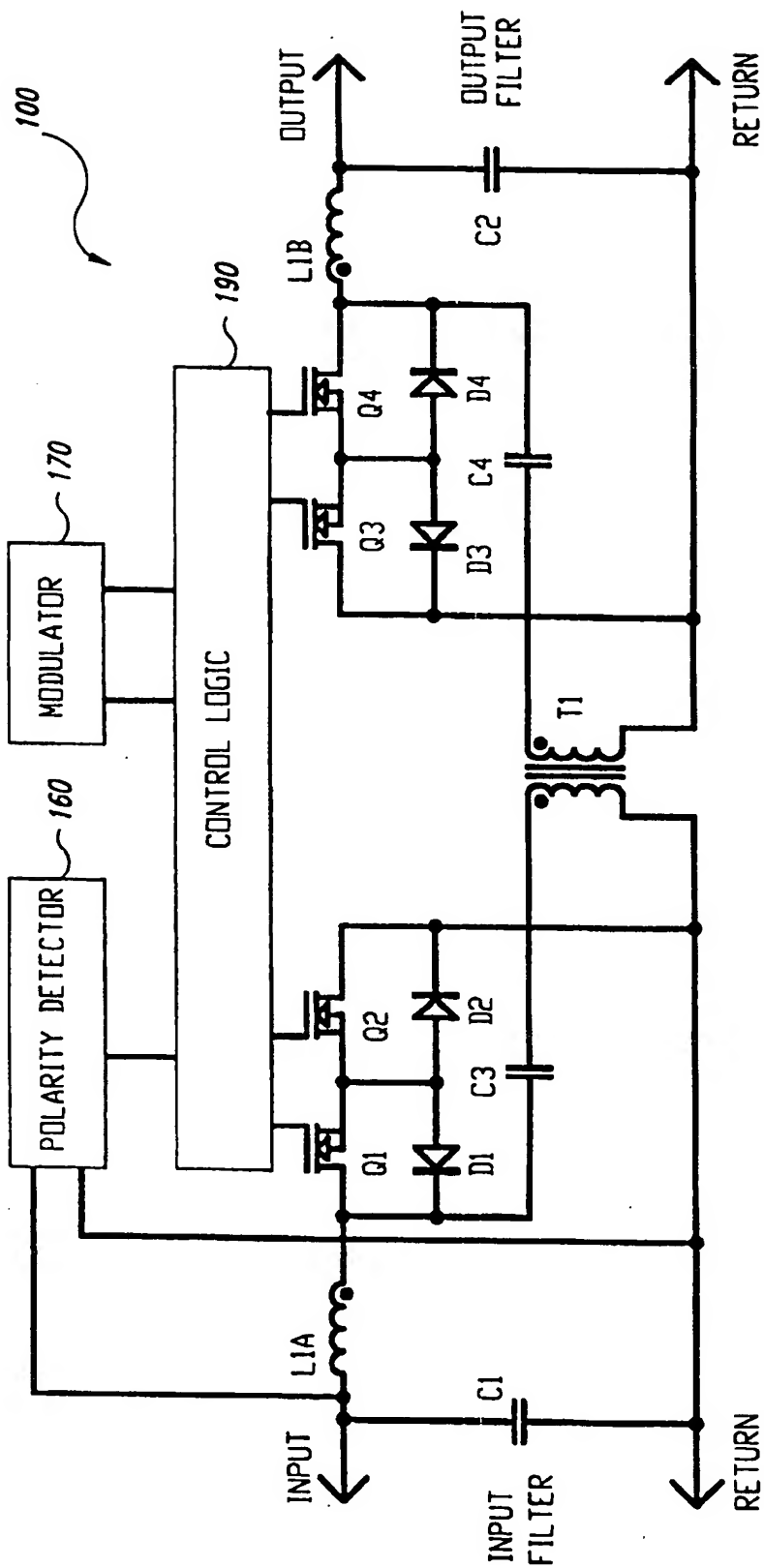


Fig. 7D

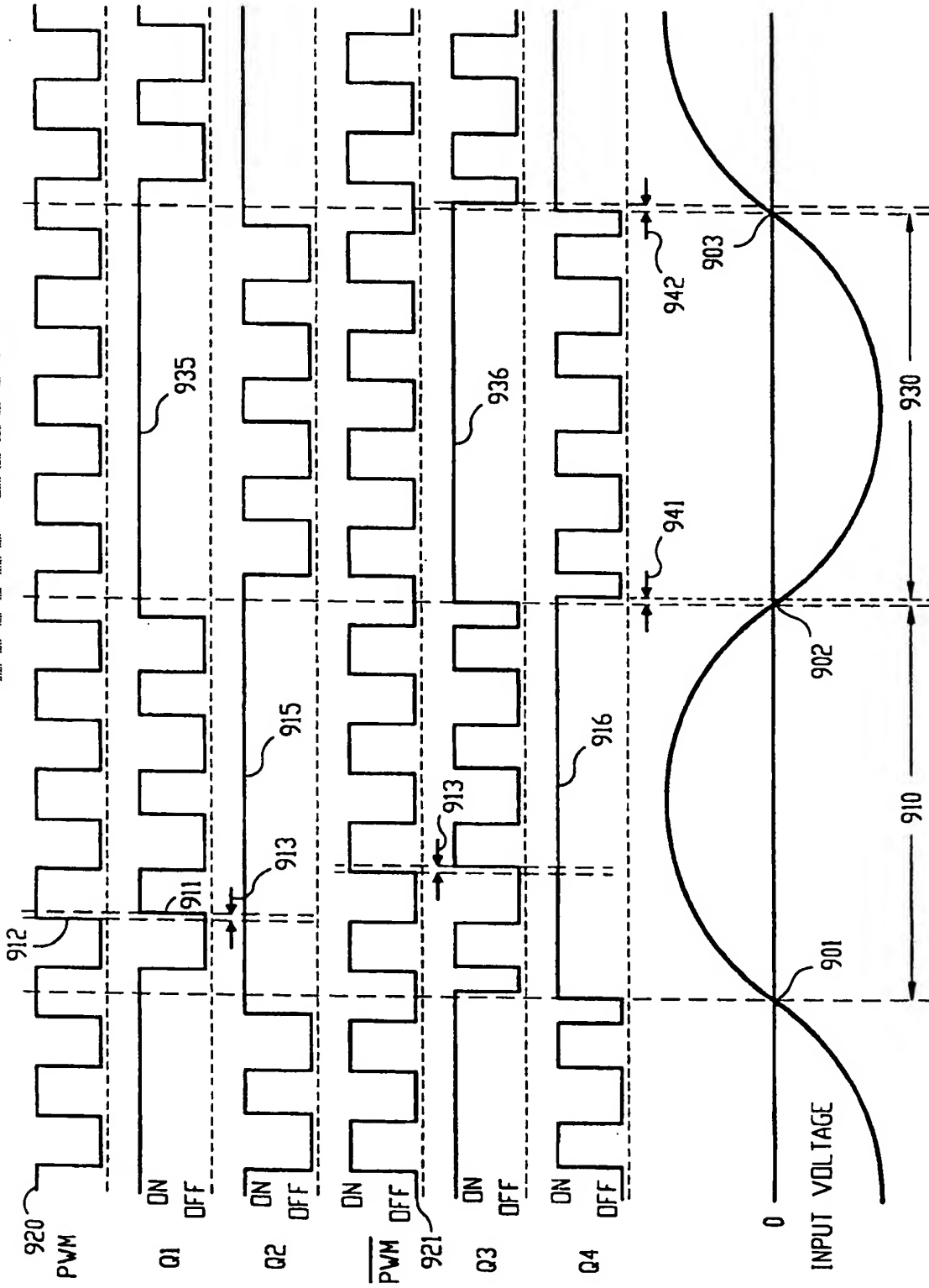


Fig. 8

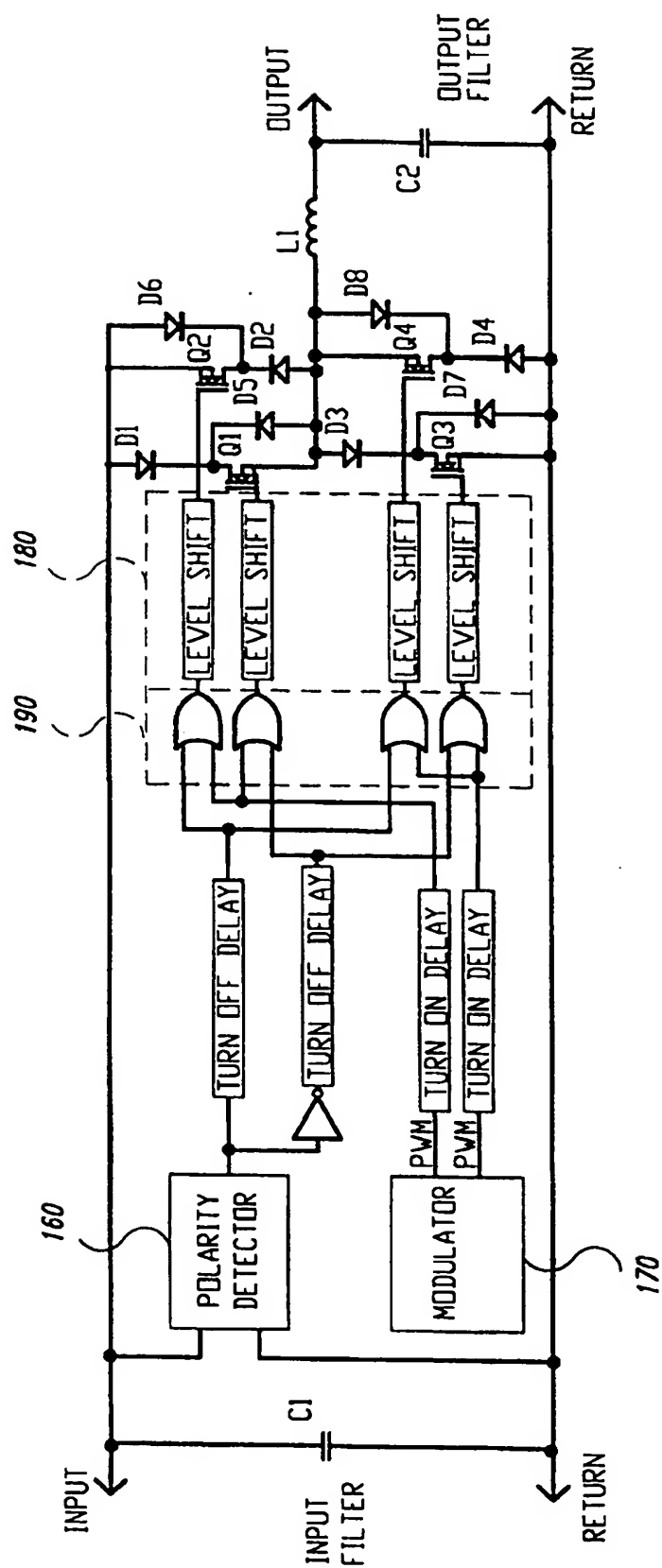


Fig. 9

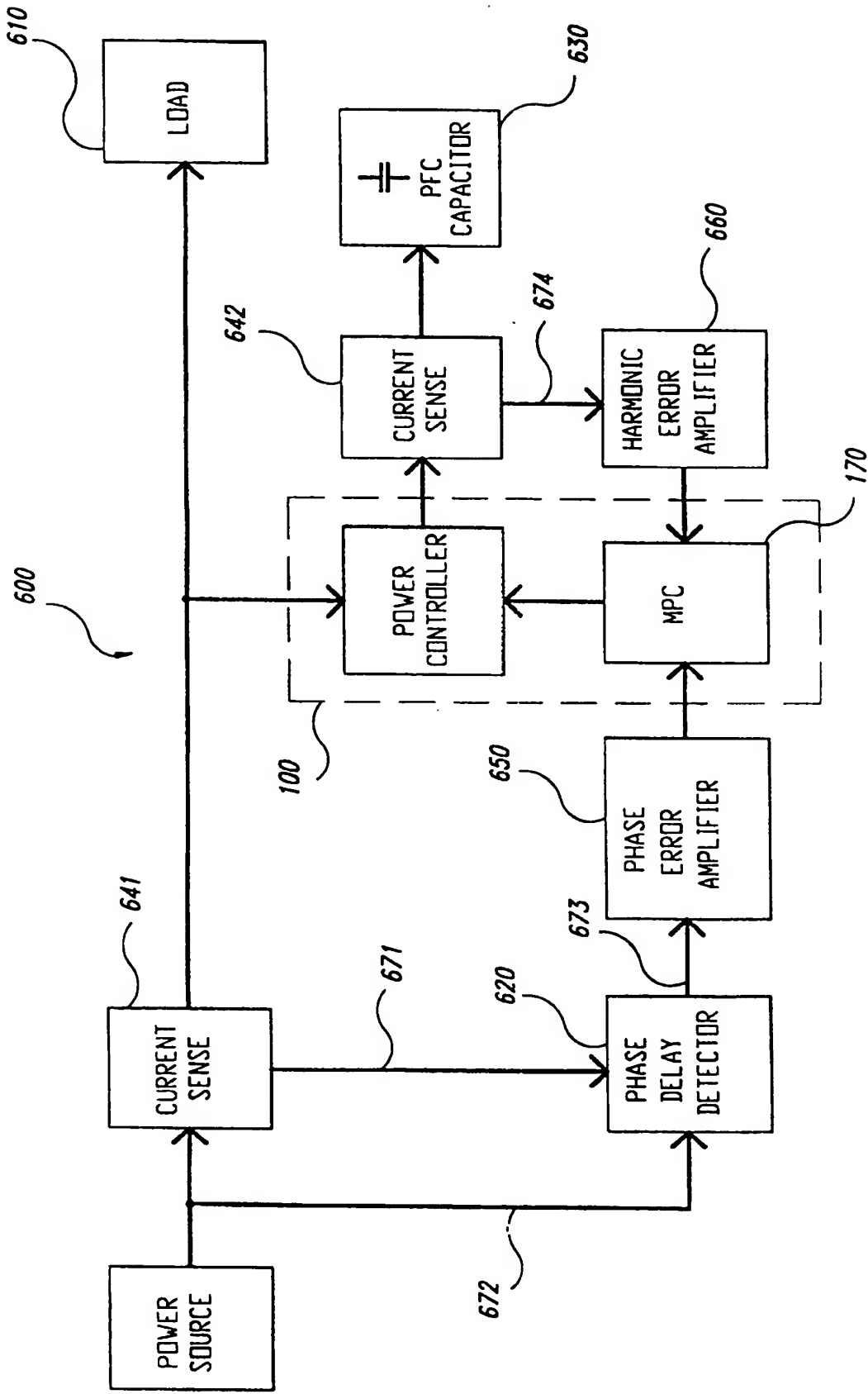


Fig. 10

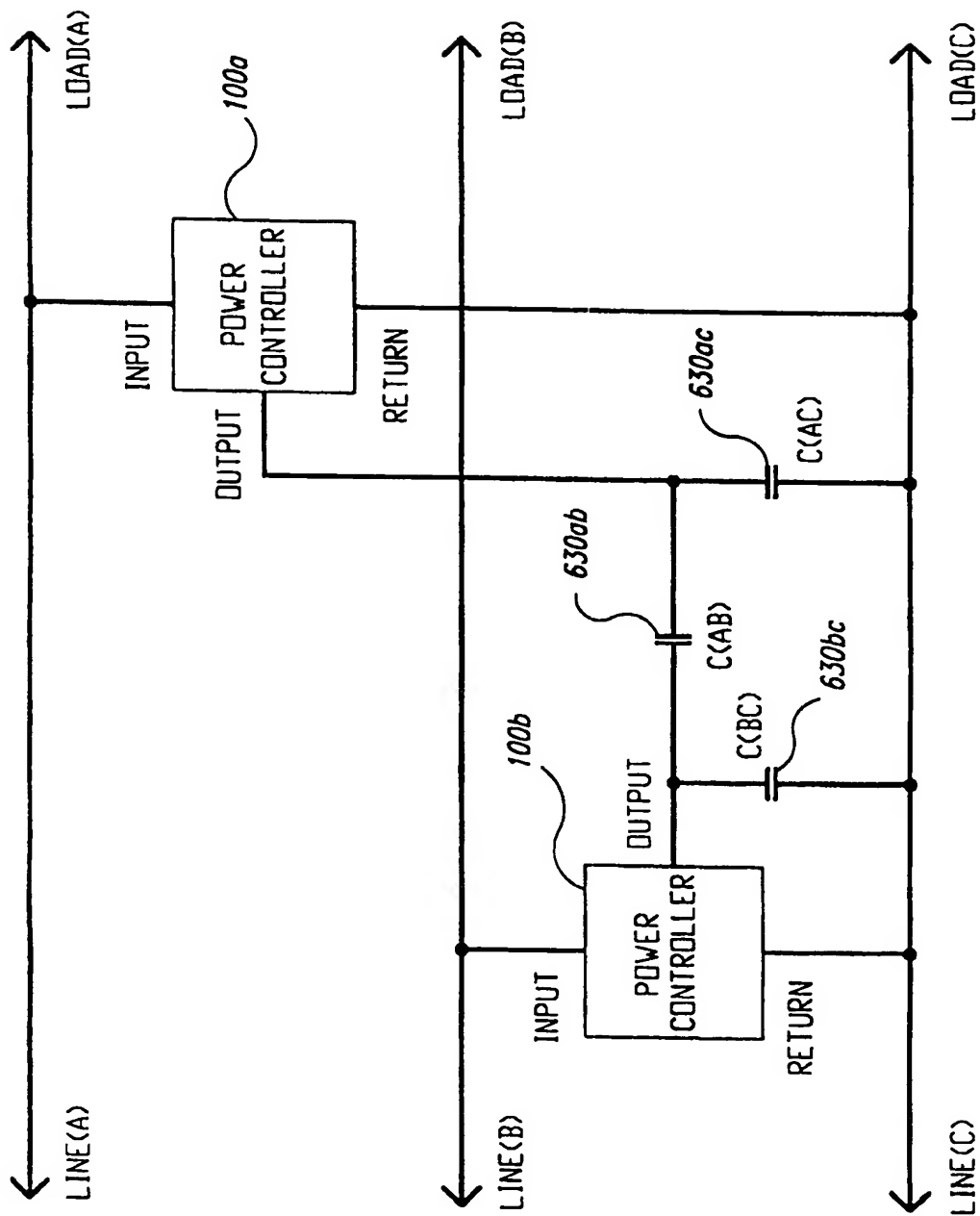


Fig. 11



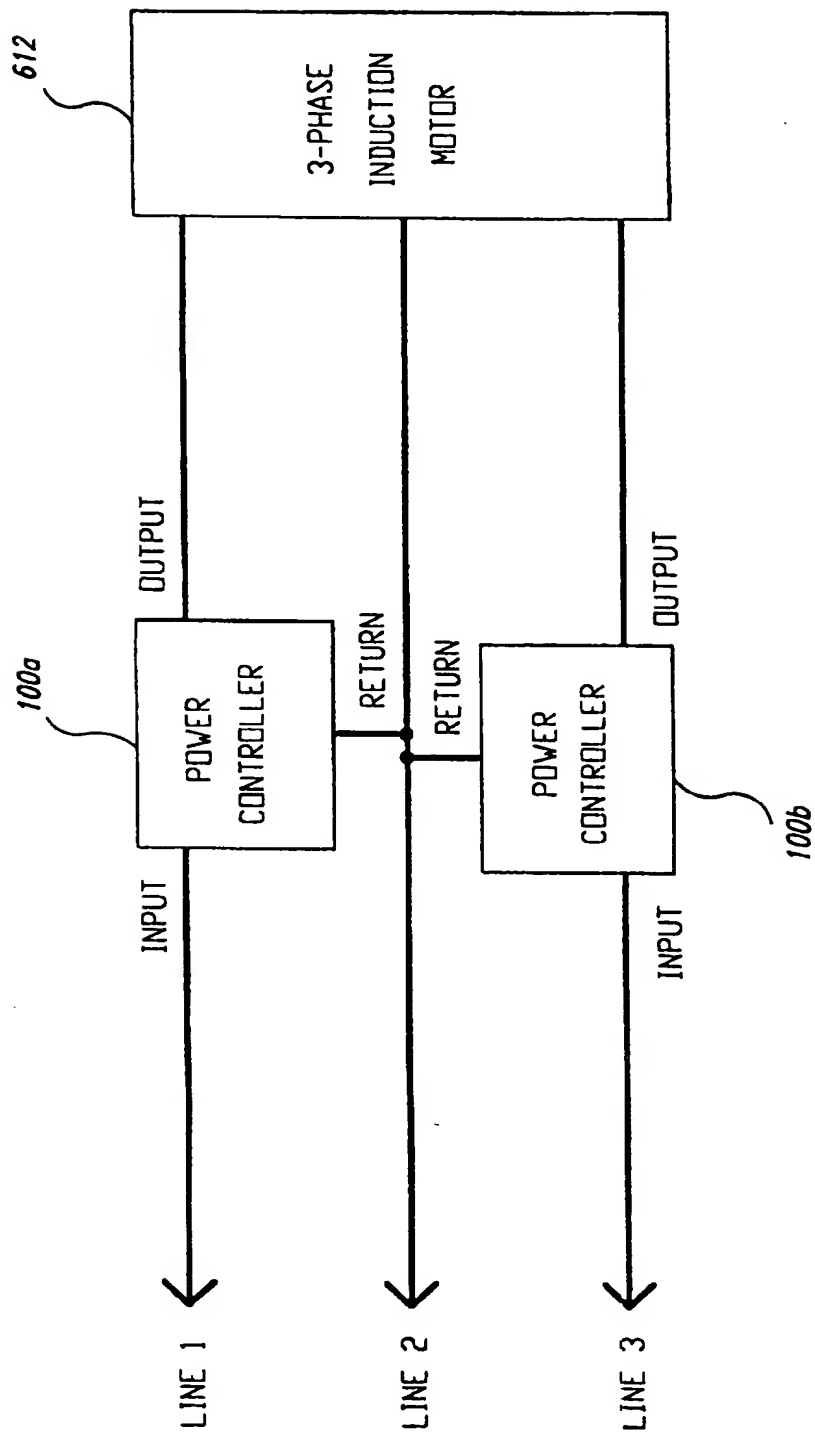
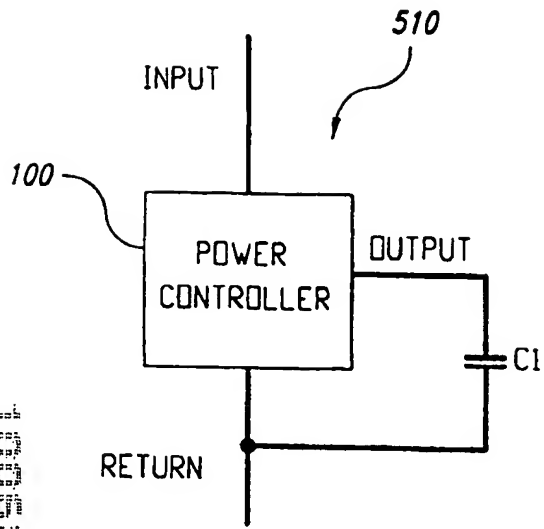
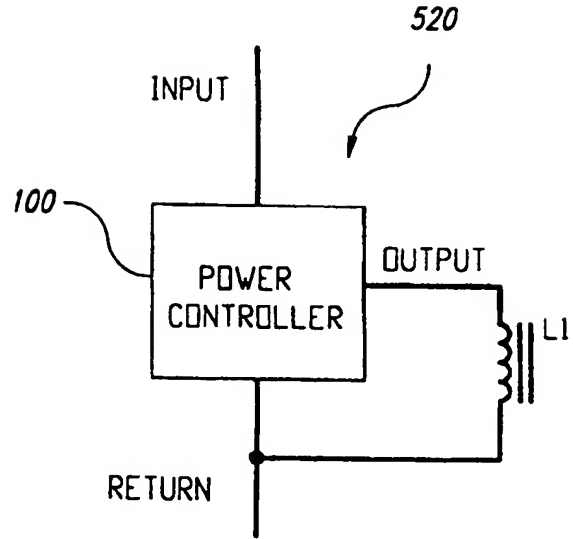


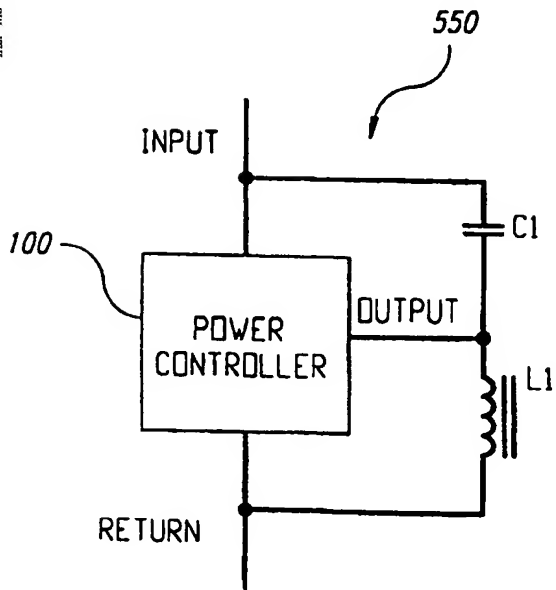
Fig. 12



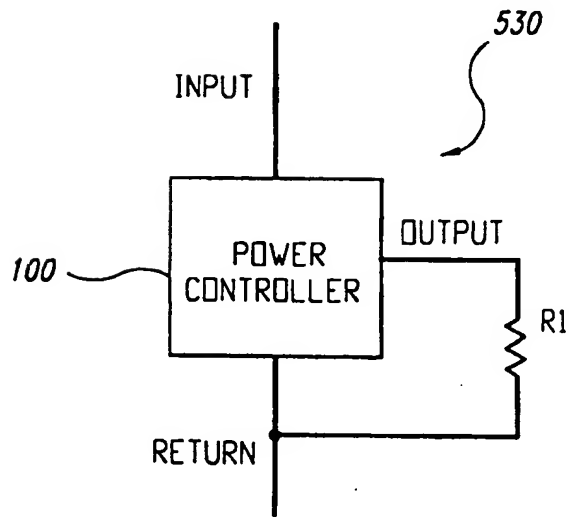
*Fig. 13*



*Fig. 14*



*Fig. 15*



*Fig. 16*

FIG. 17 is a schematic diagram of a power controller 100 in a first state. The power controller 100 is connected to an input 702 and an output 704. The input 702 is labeled "INPUT HIGH" and the output 704 is labeled "OUTPUT LOW". The power controller 100 has an "IN" terminal and a "RETURN" terminal. The "IN" terminal is connected to the input 702 and the "RETURN" terminal is connected to the output 704. The power controller 100 is shown in a first state where the output 704 is low.

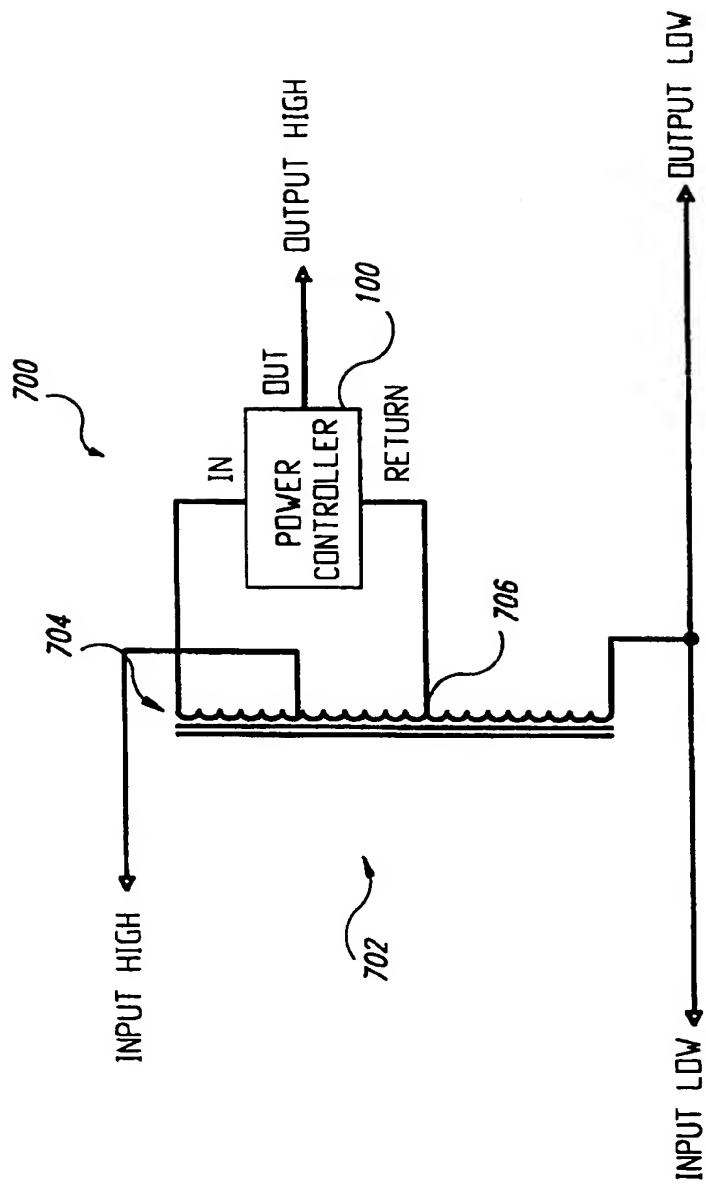


Fig. 17

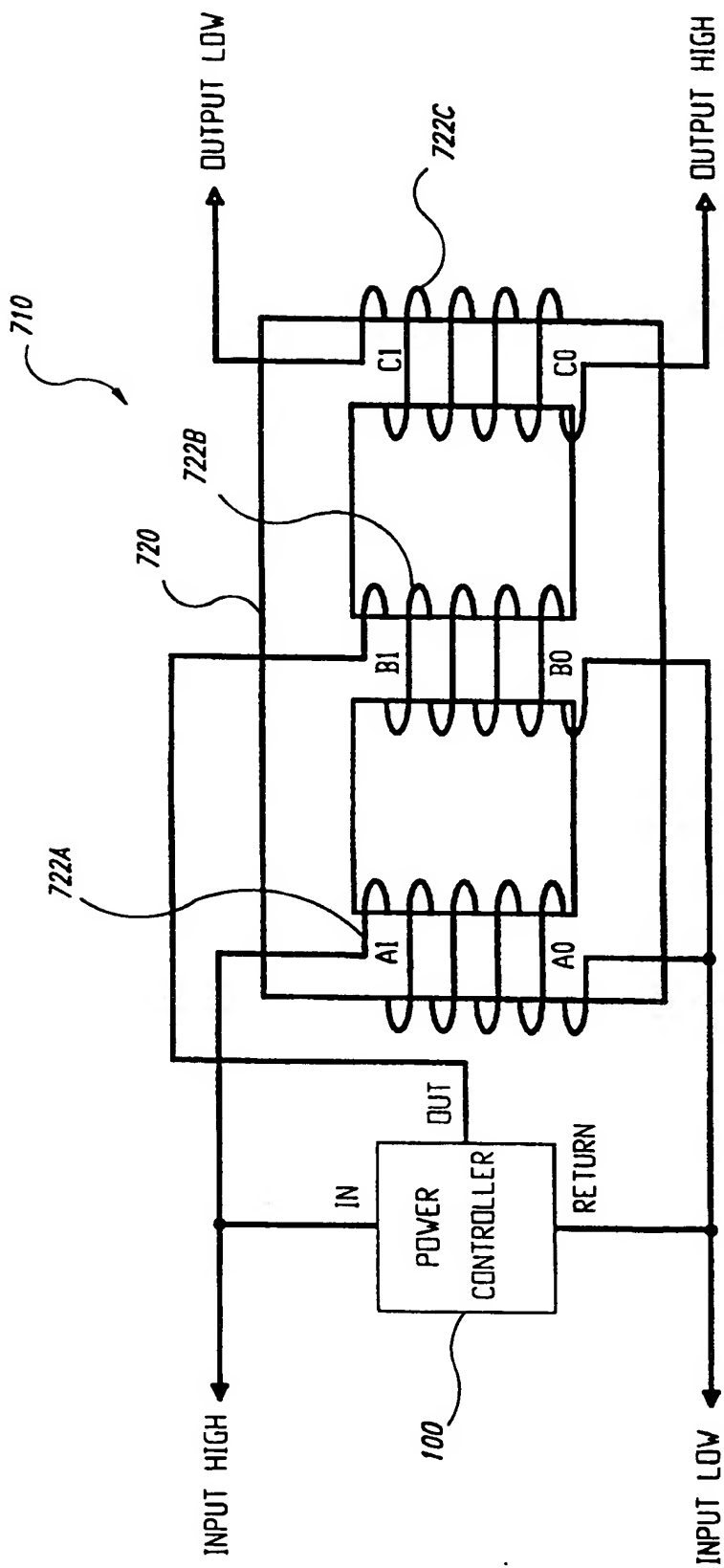


Fig. 18

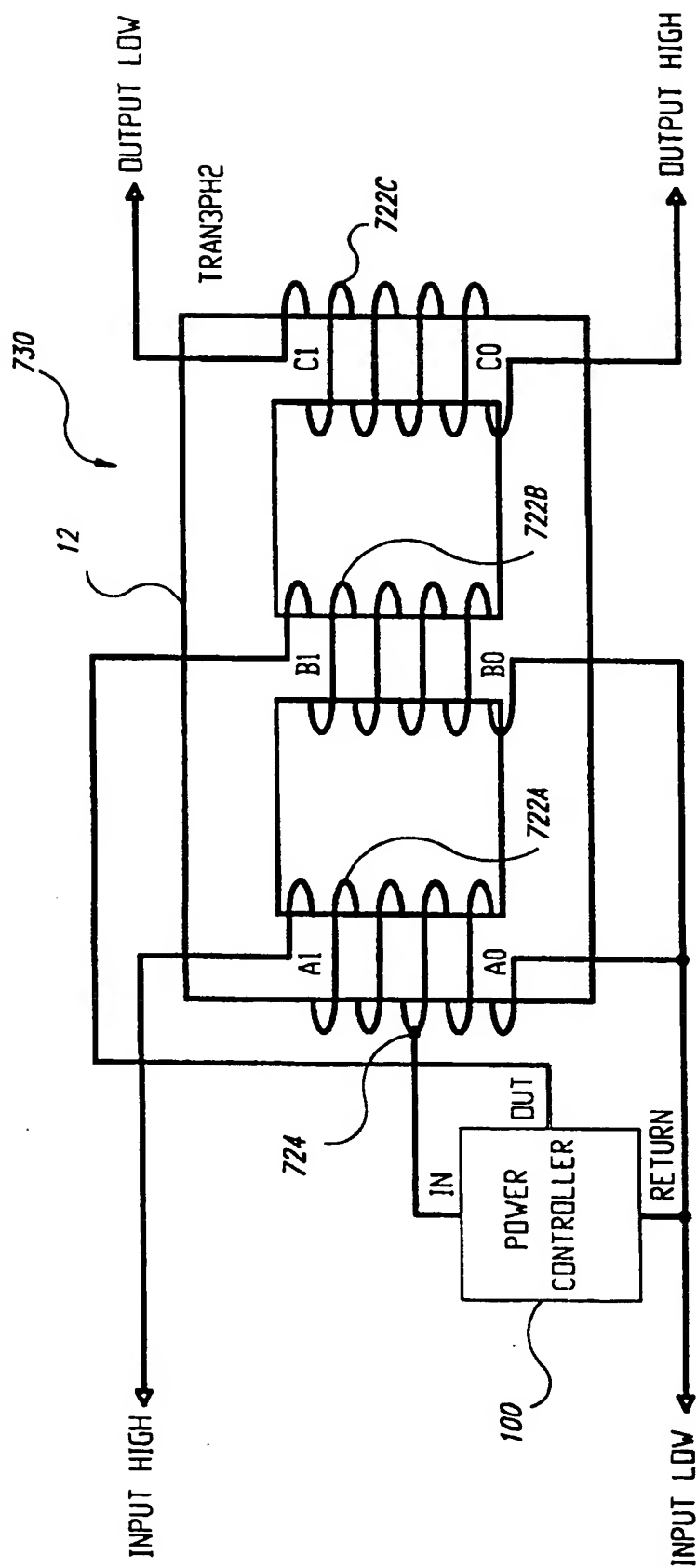


Fig. 19

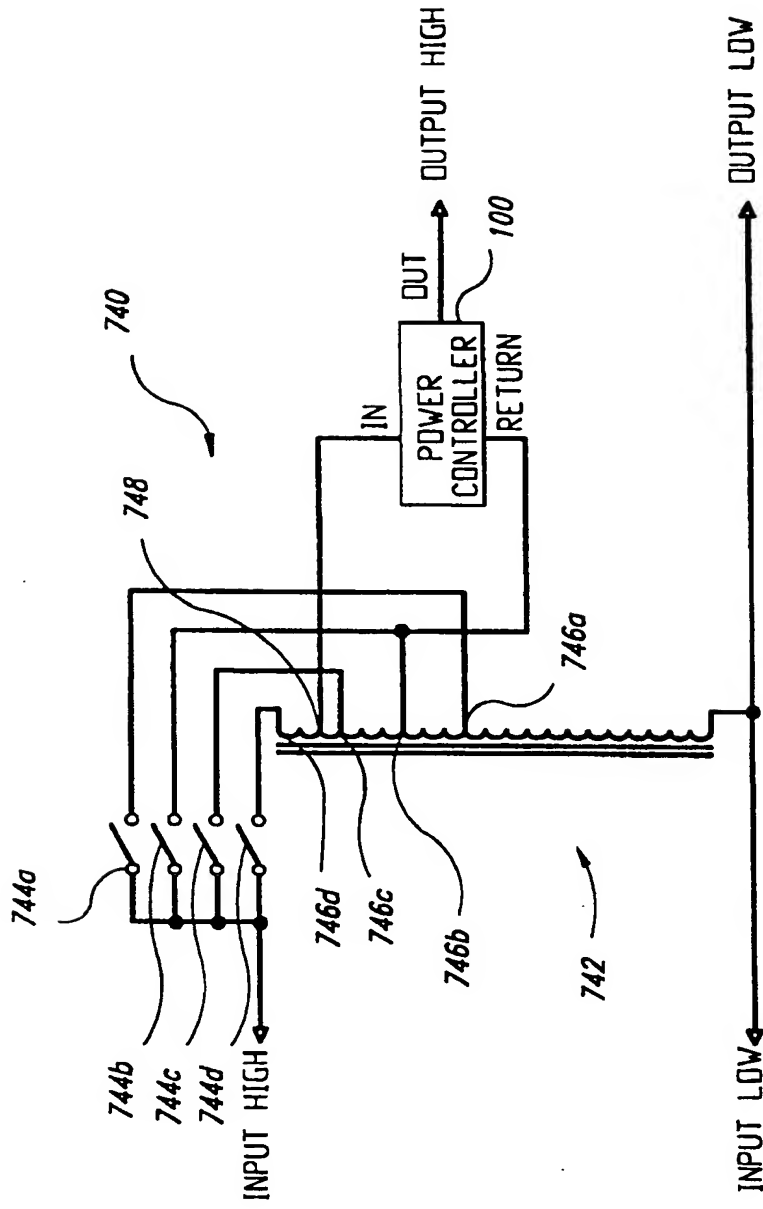


Fig. 20

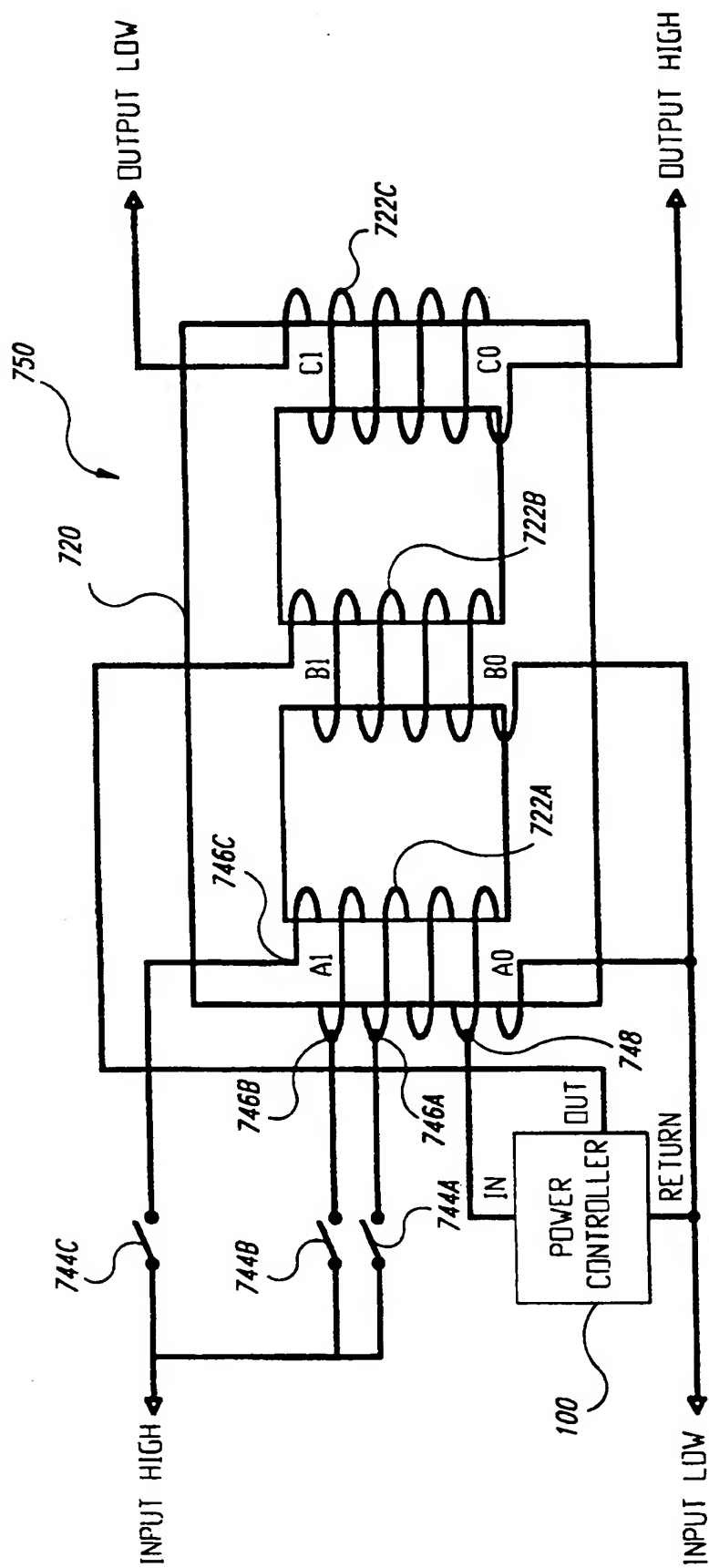


Fig. 21

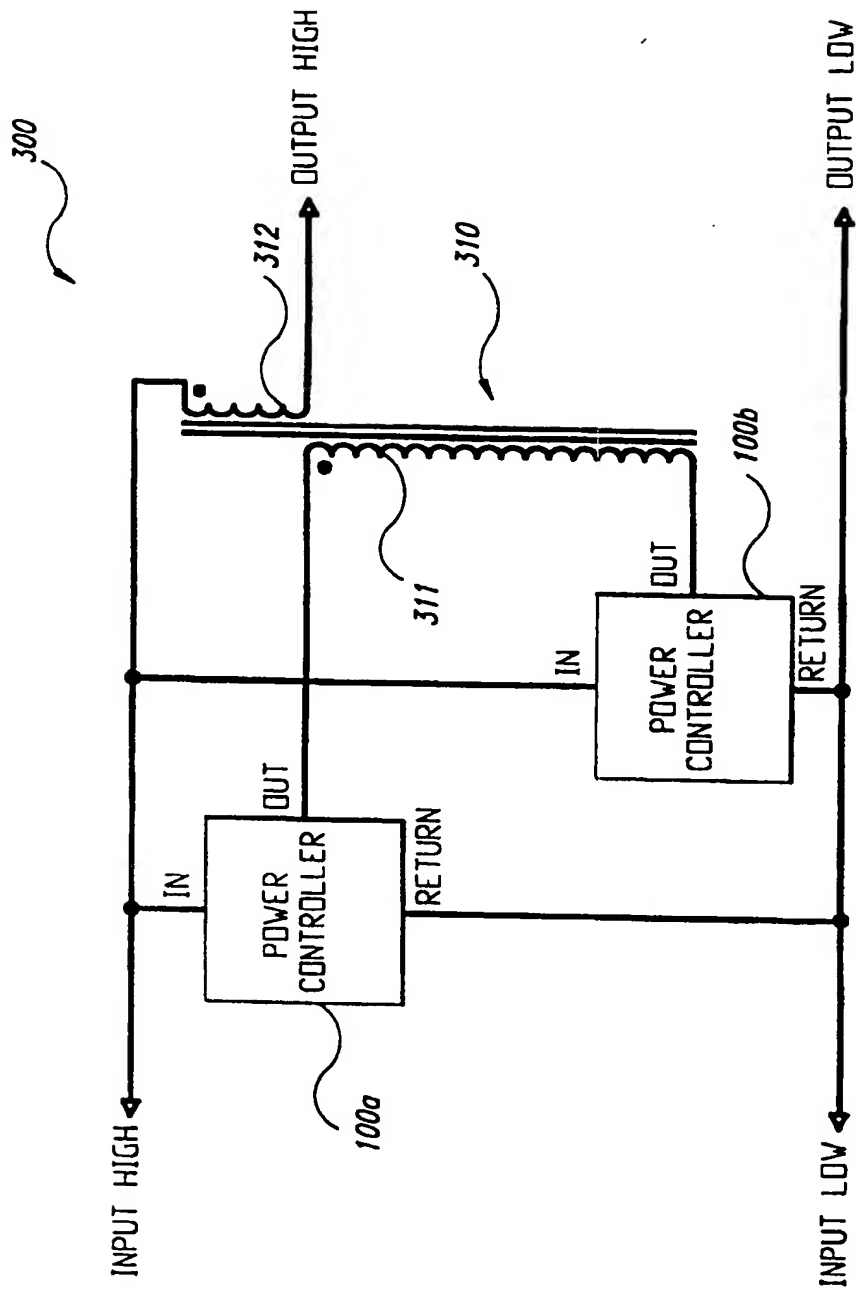


Fig. 22



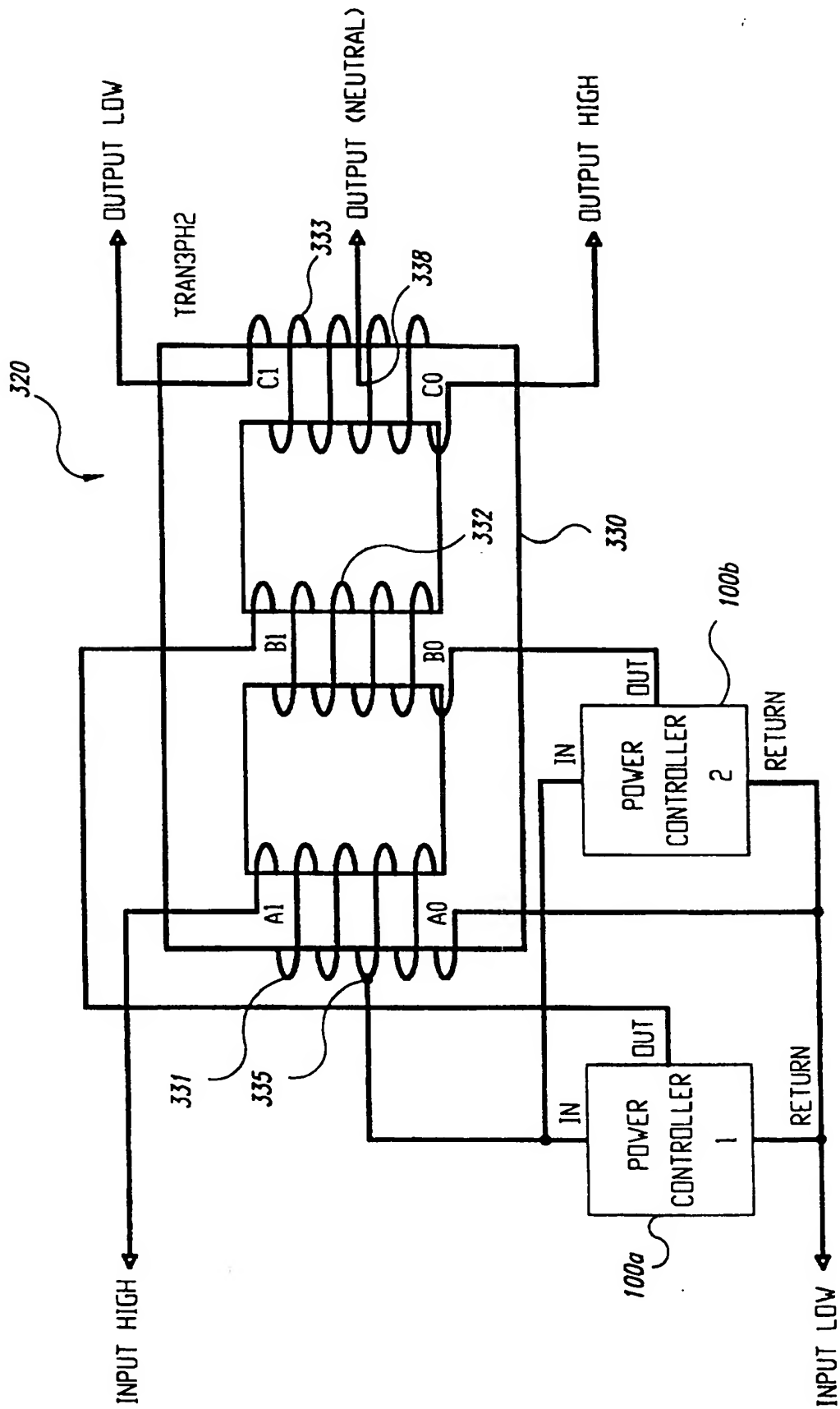


Fig. 23

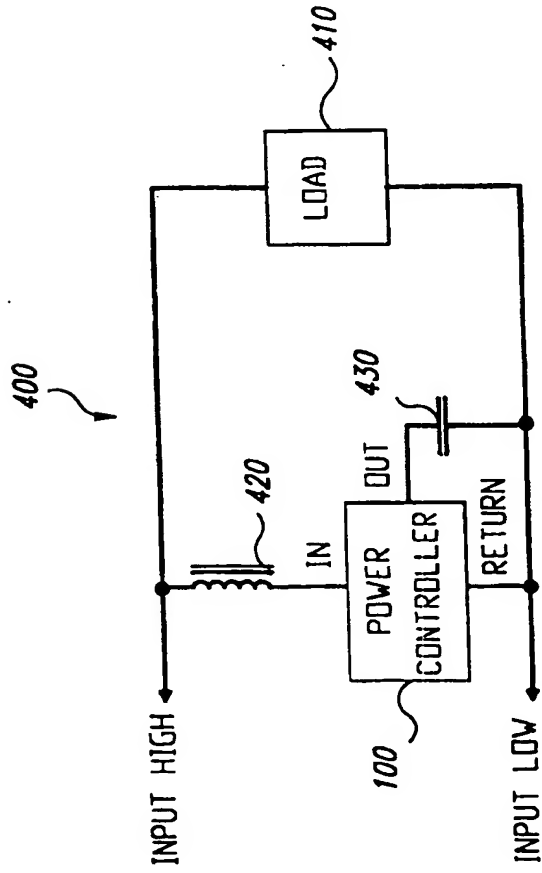


Fig. 24

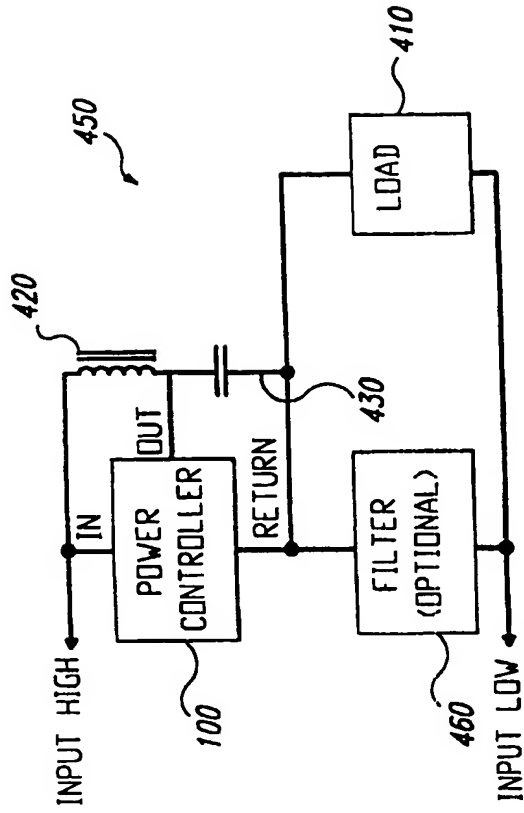


Fig. 25

0.00000 s  
5.00 ms/div  
25.0000 ms

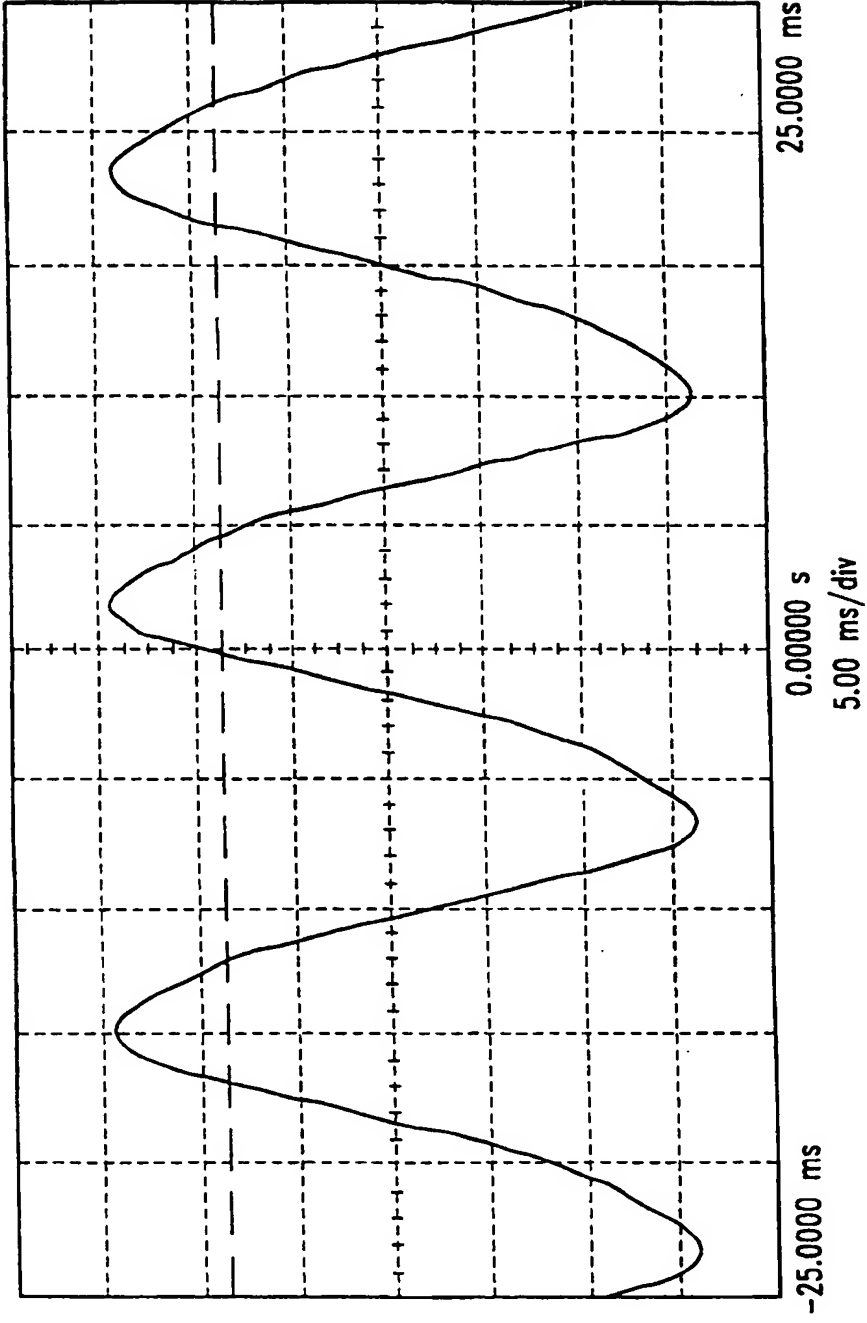


Fig. 26A

**Fig. 26B**

0.00000 s  
5.00 ms/div

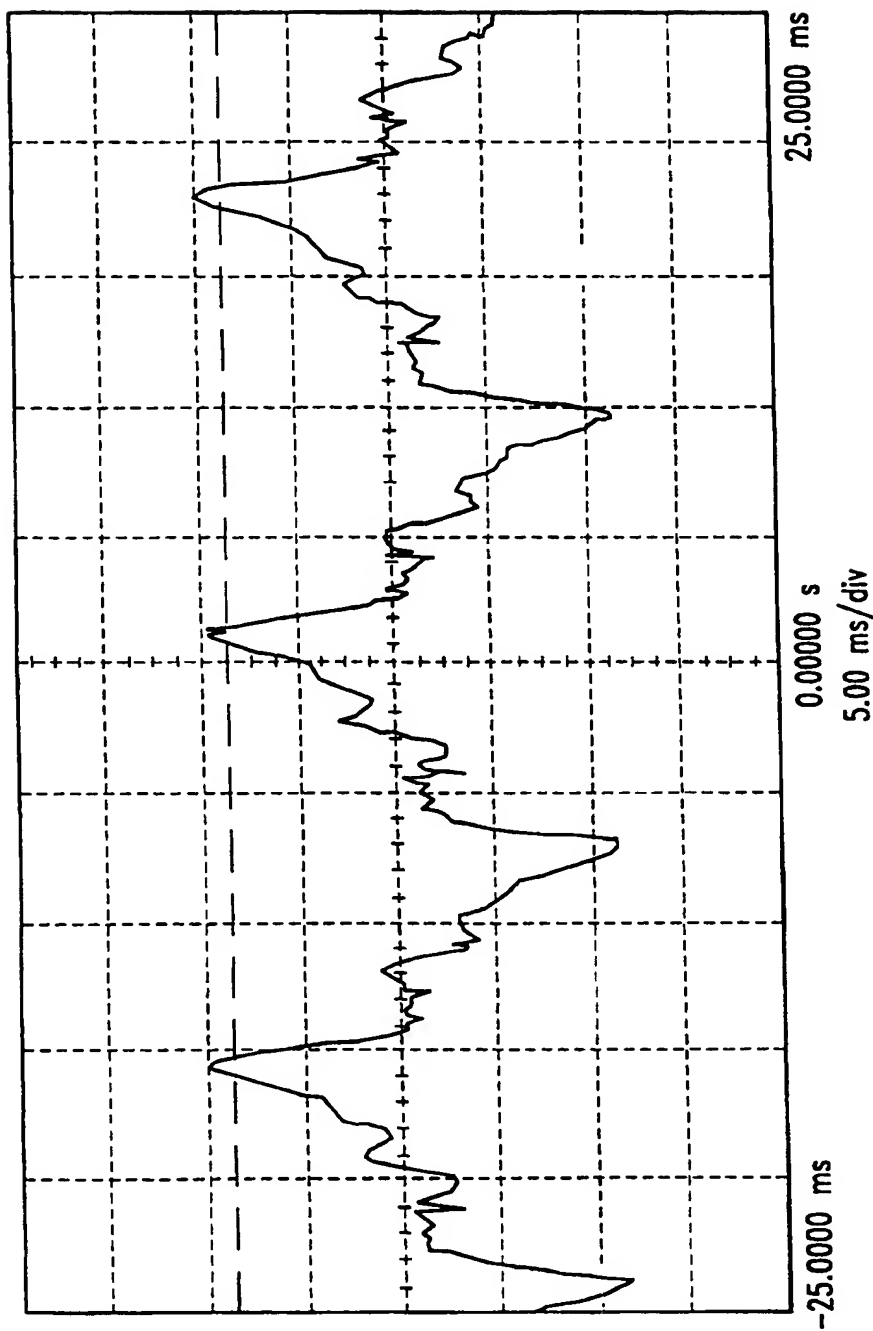


Fig. 26C

0.00000 s  
5.00 ms/div  
25.0000 ms

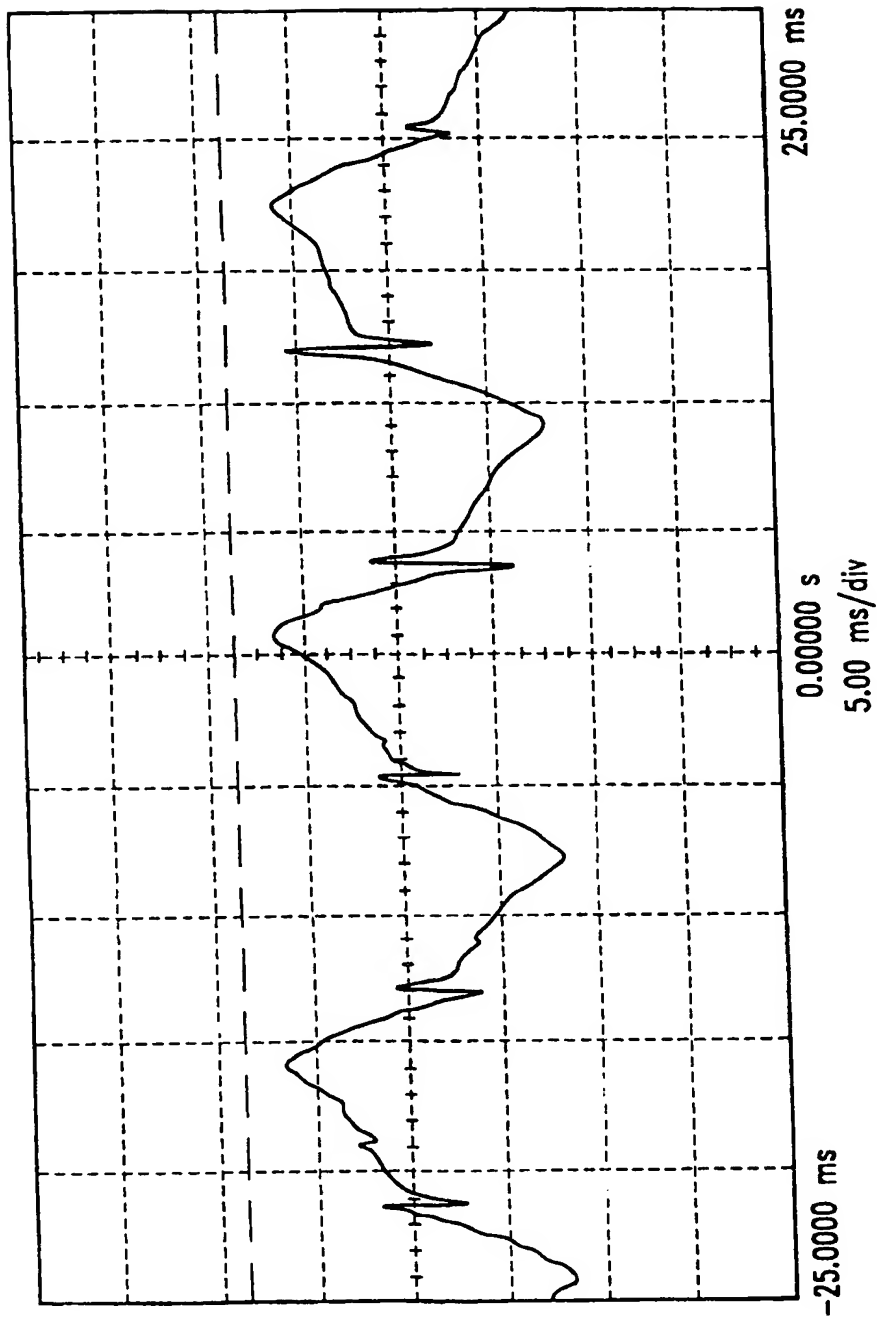


Fig. 26D

0.0000 s  
5.00 ms/div  
25.0000 ms

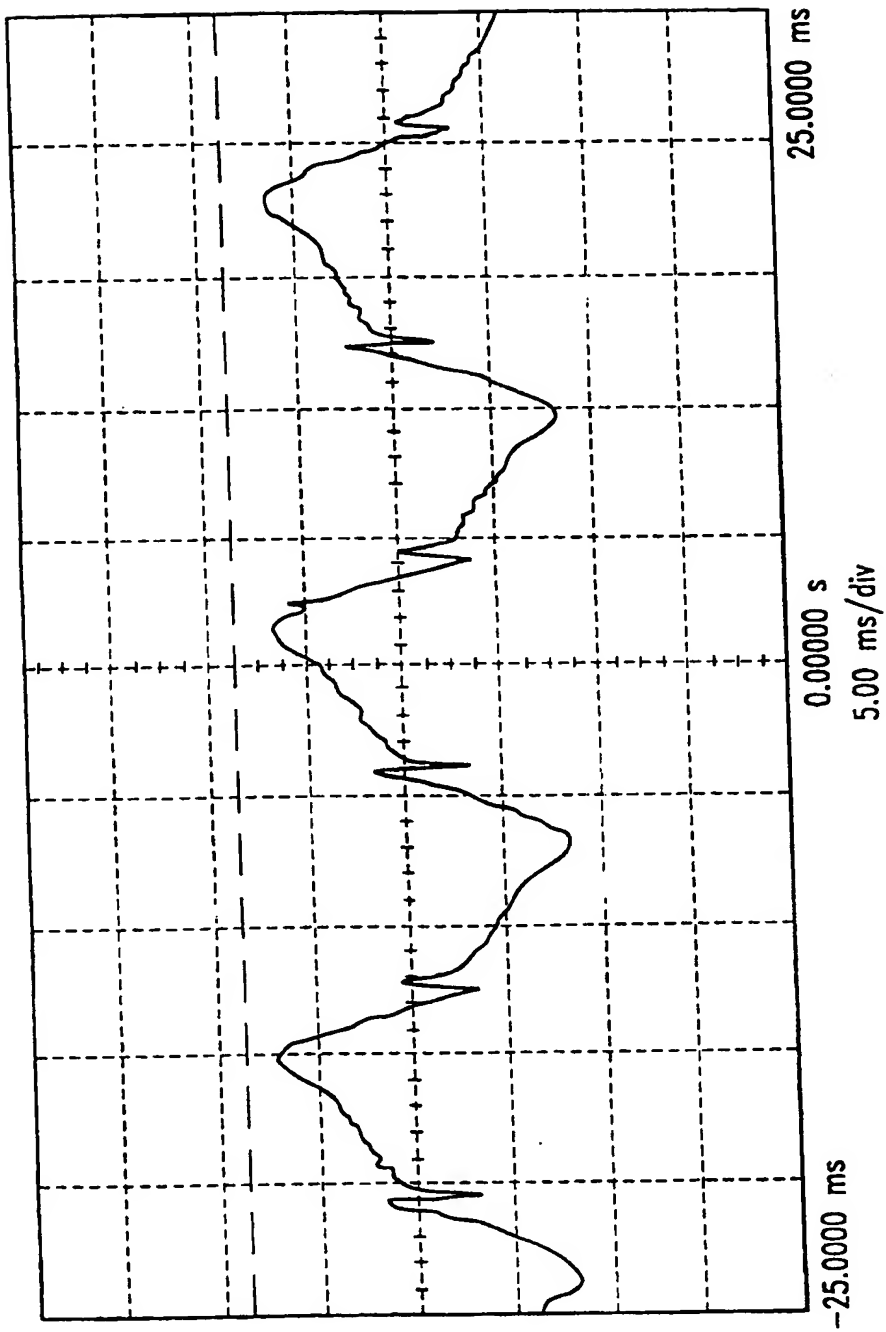


Fig. 26E

Fig. 27

[illegible]



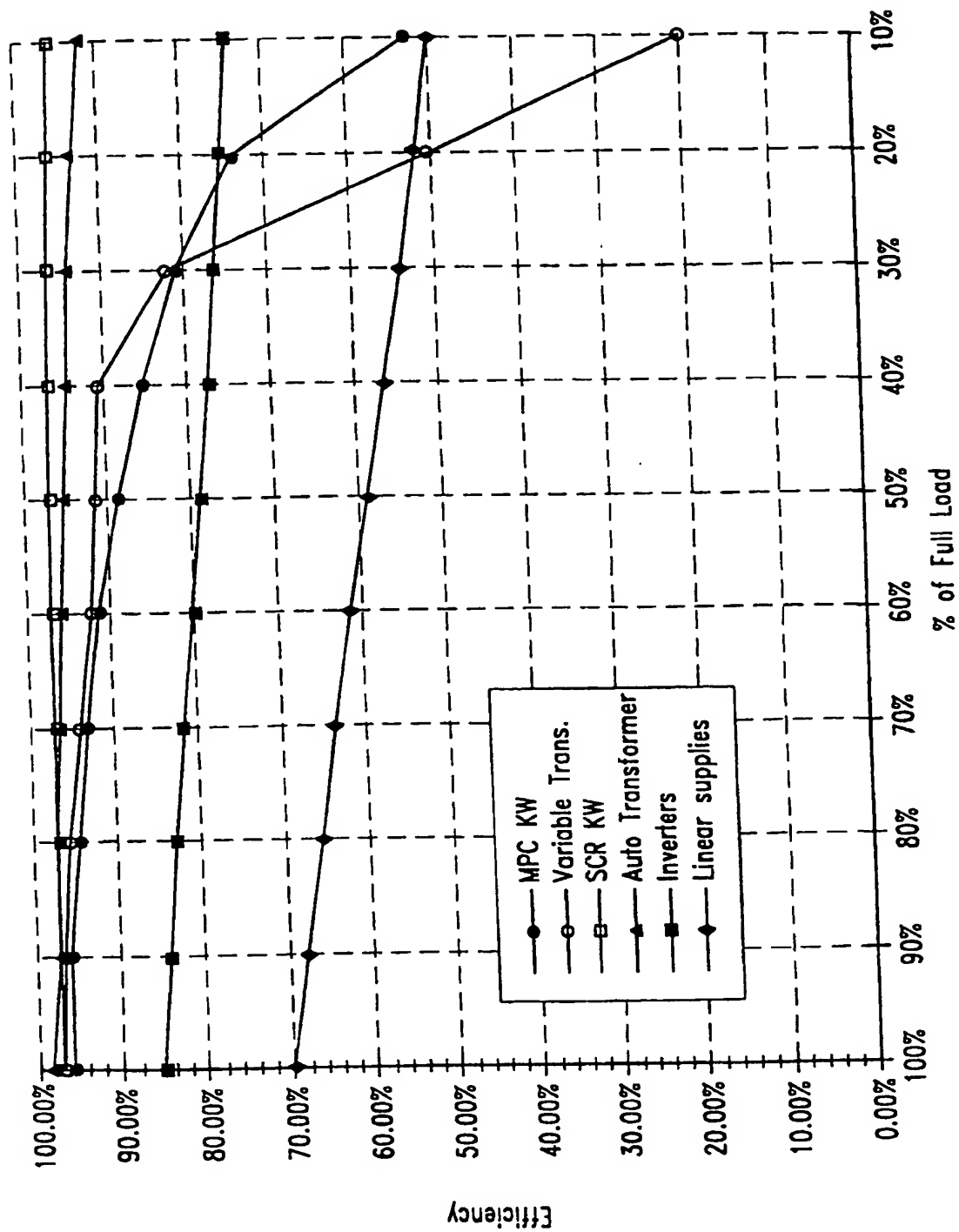


Fig. 28

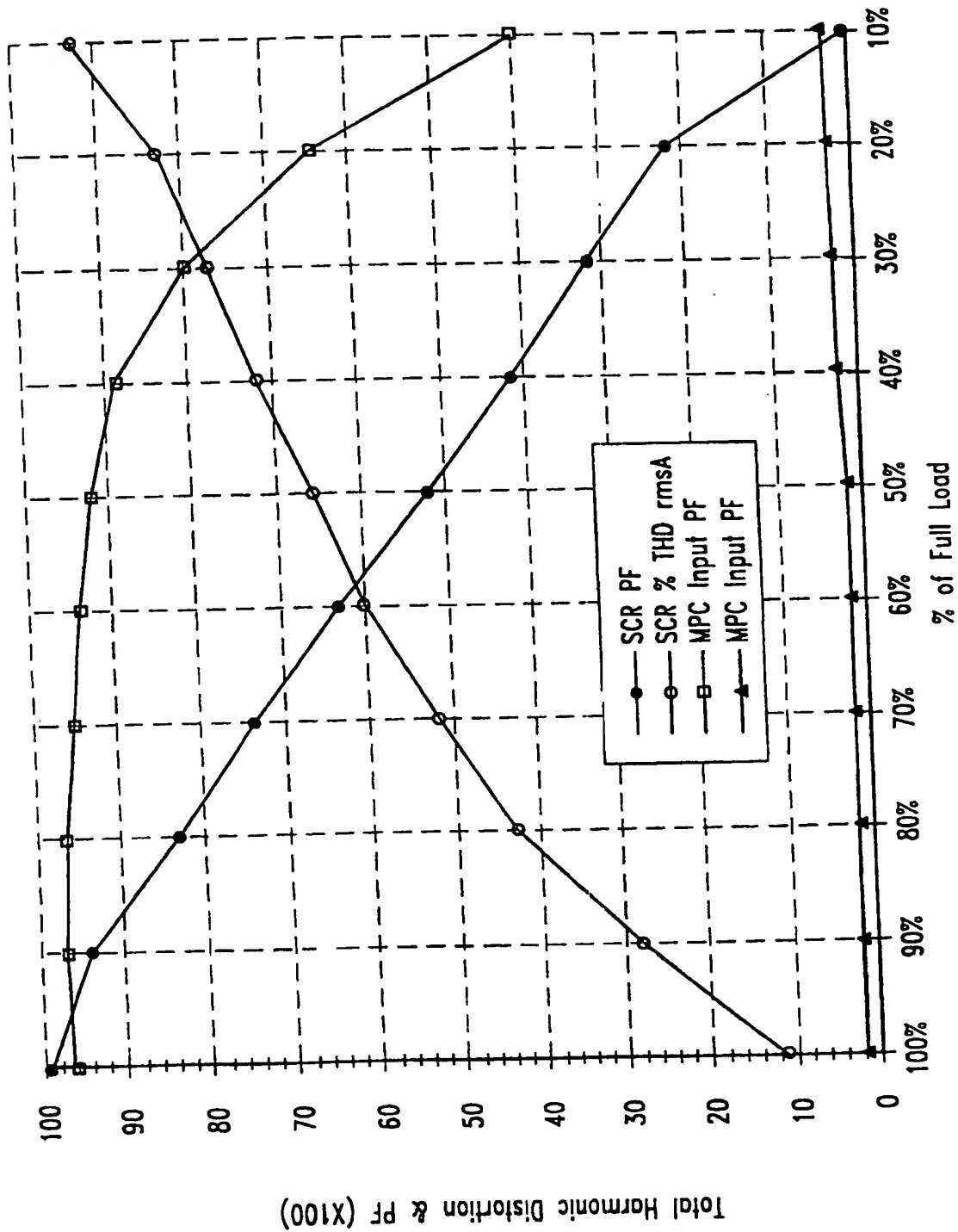


Fig. 29

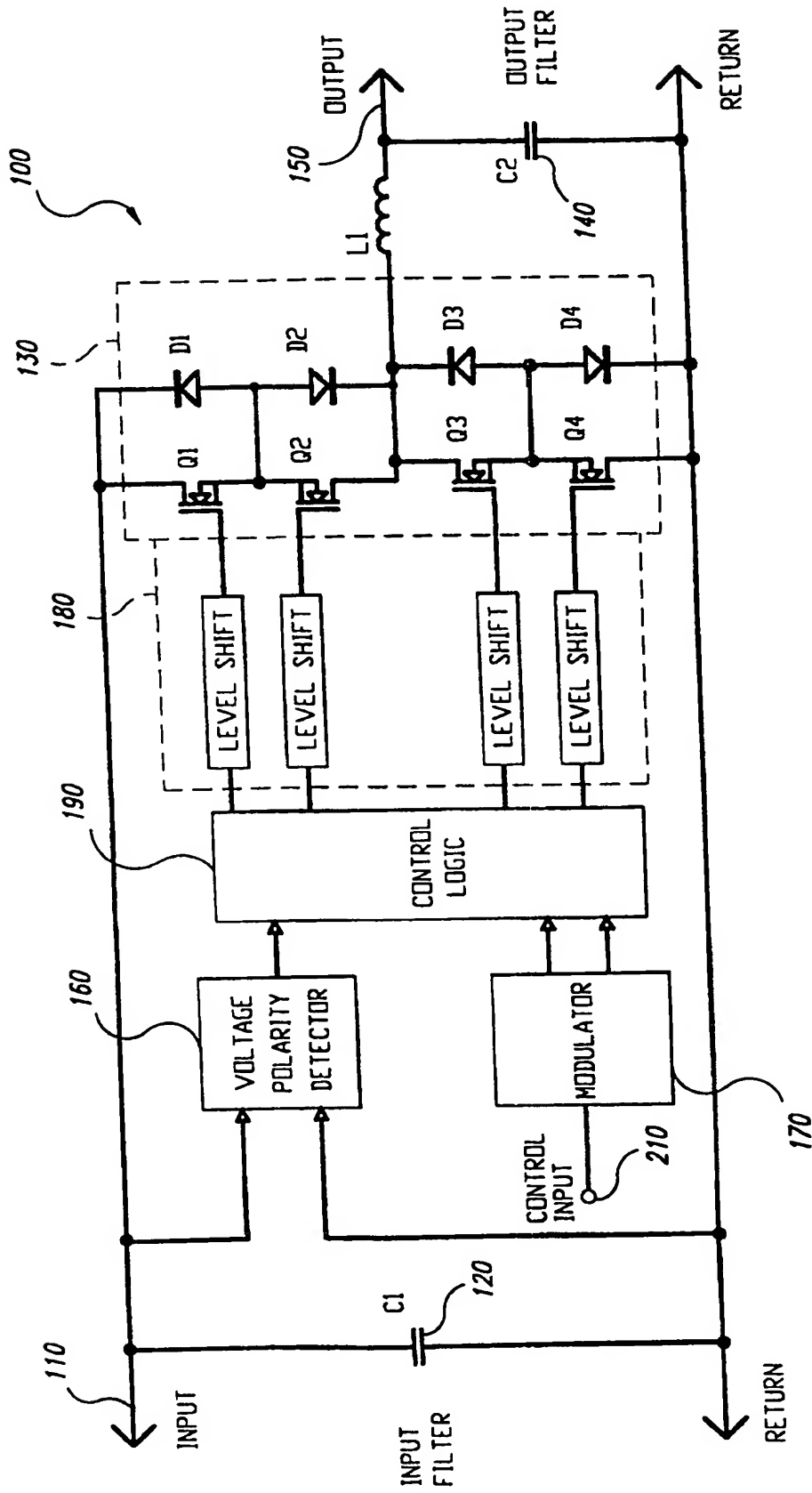


Fig. 30

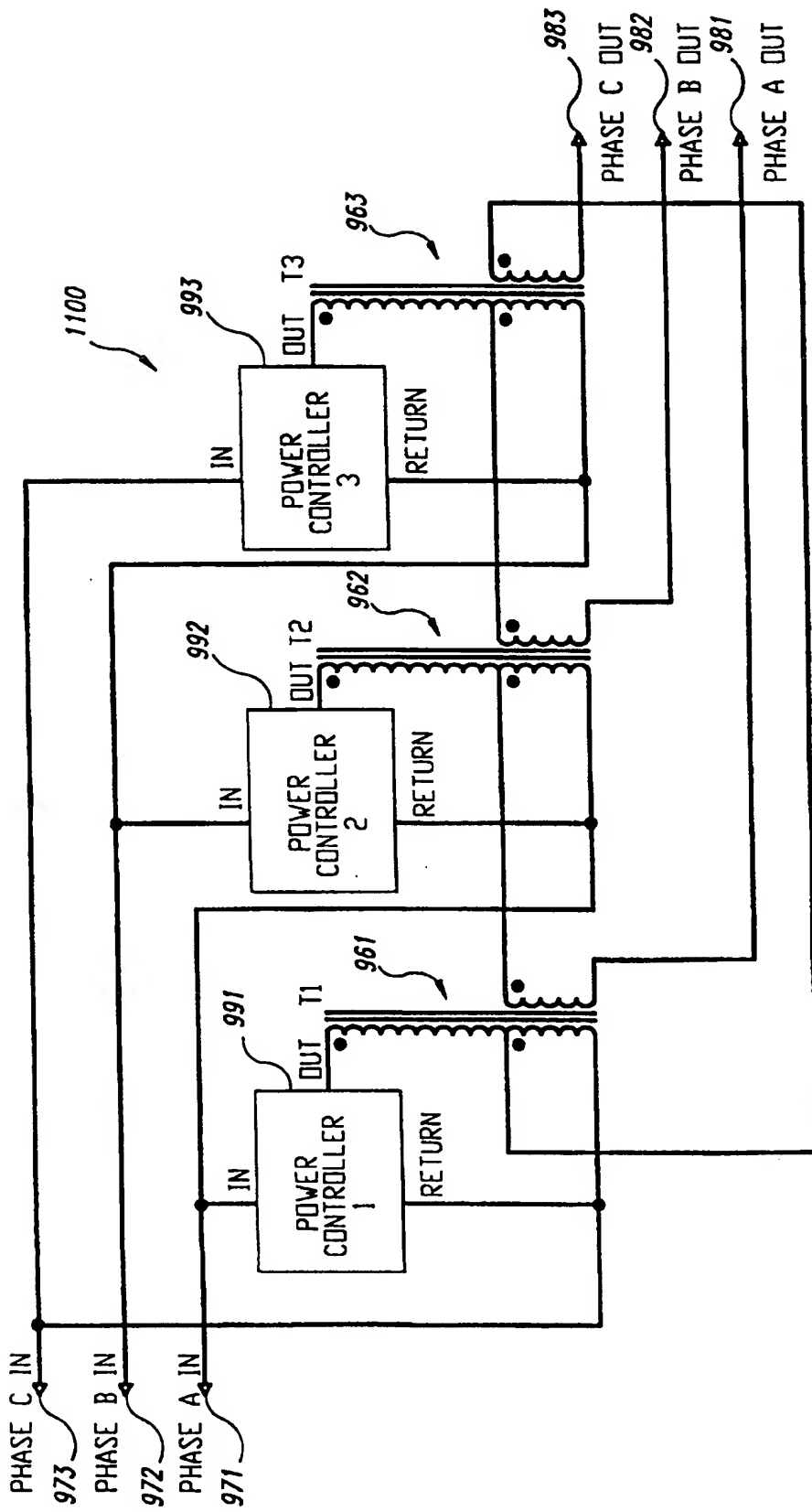
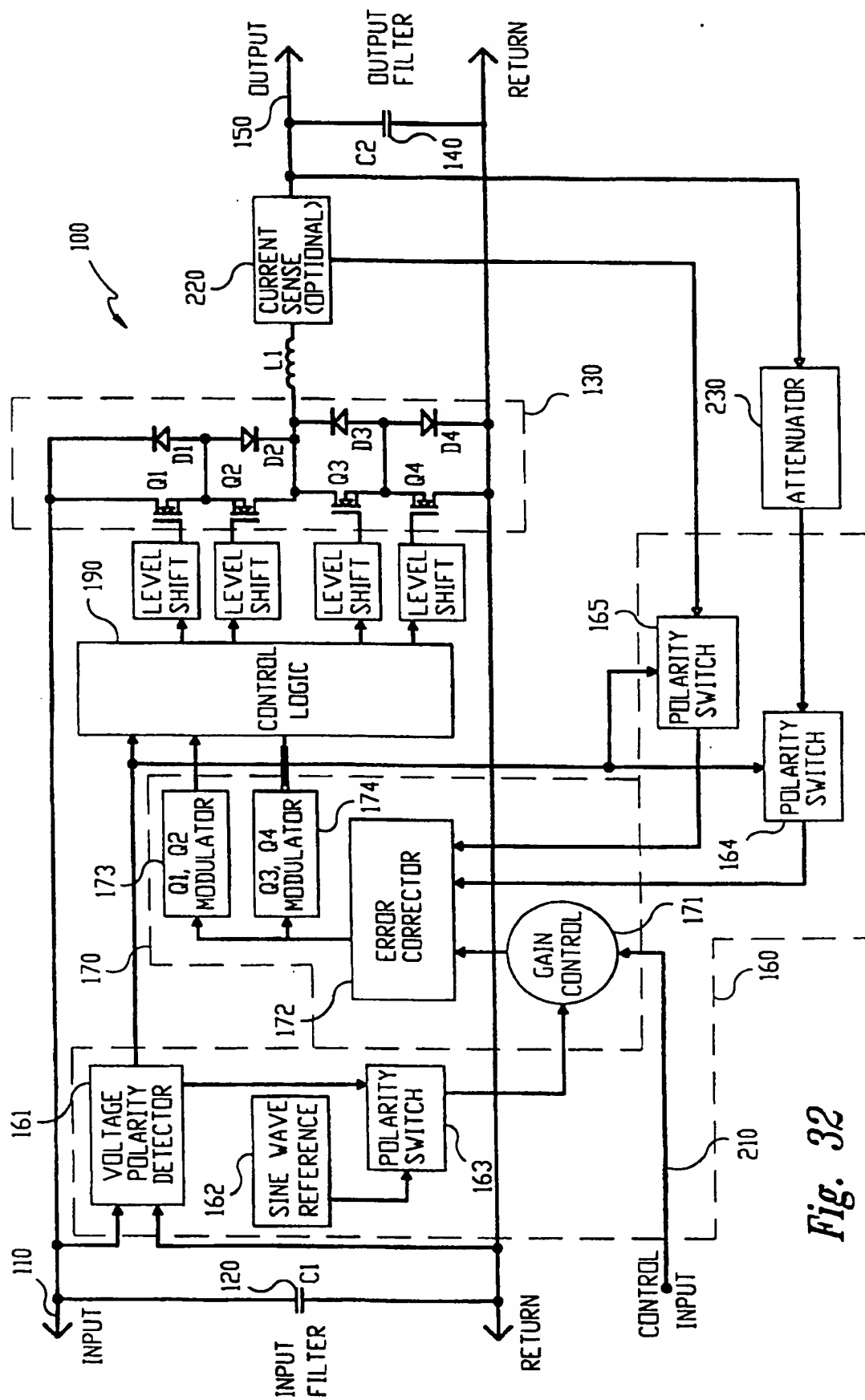


Fig. 31



**Fig. 32**

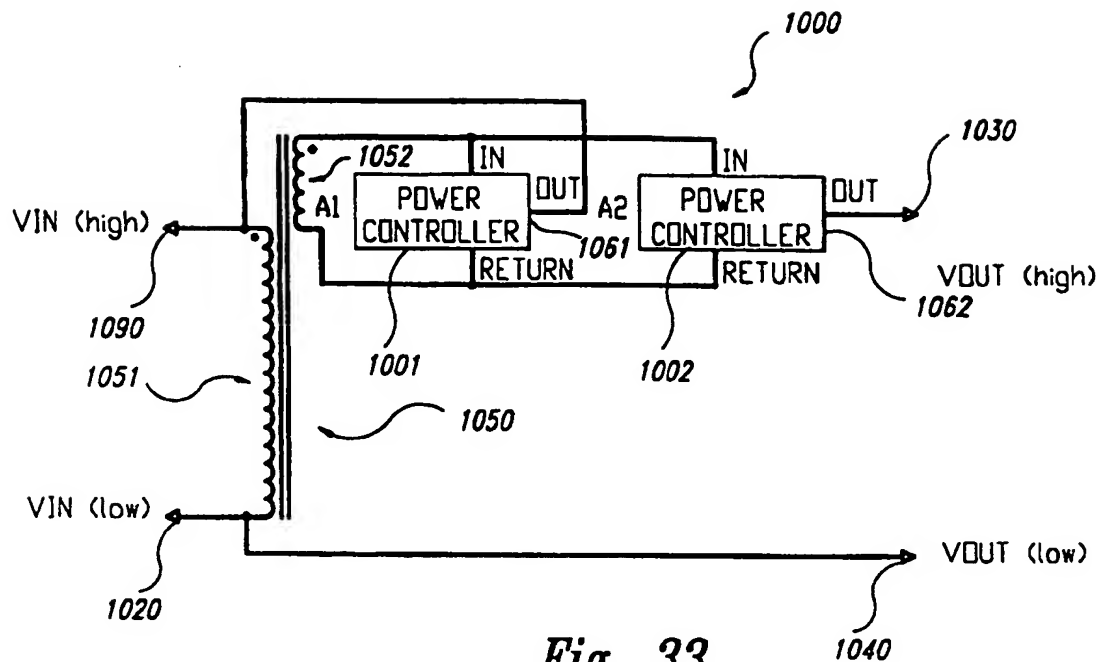


Fig. 33

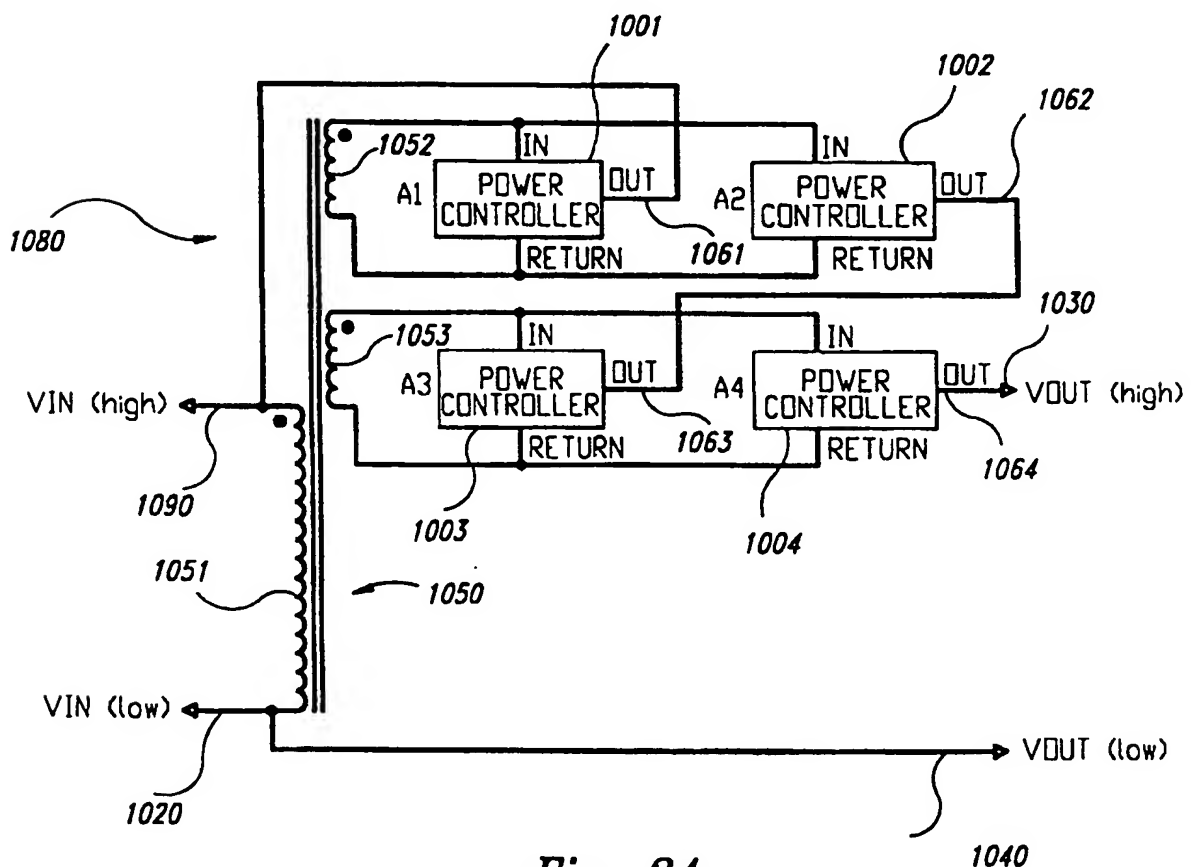


Fig. 34

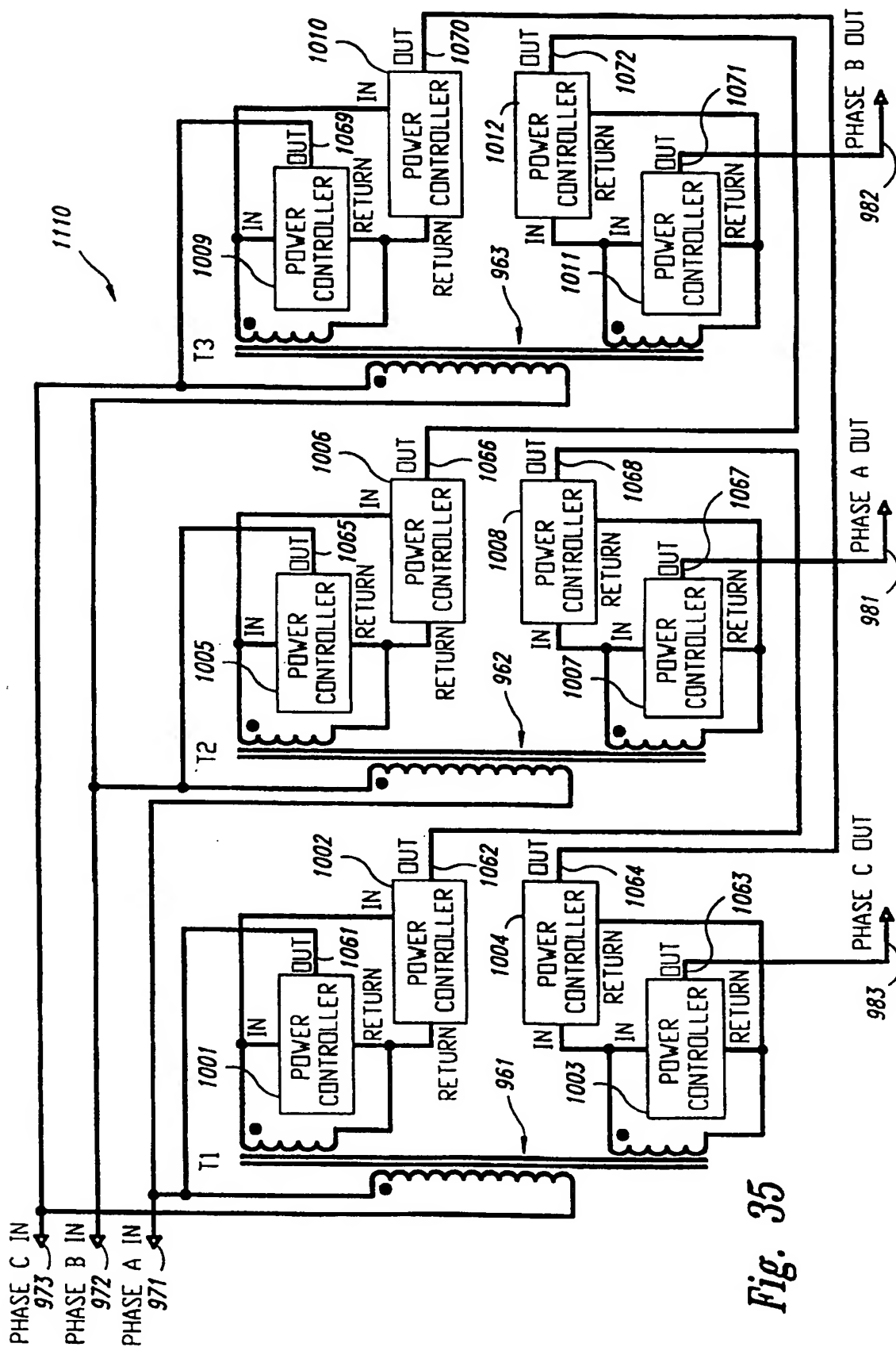


Fig. 35